FIG. 1

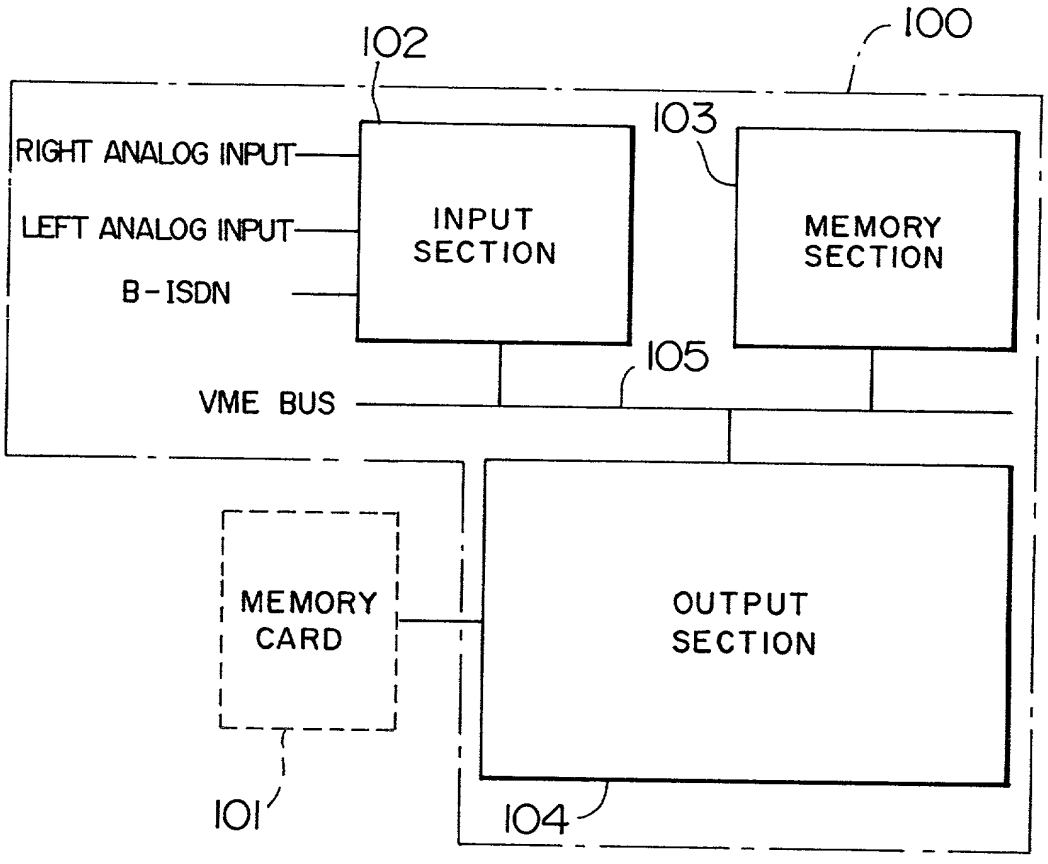

FIG. 2

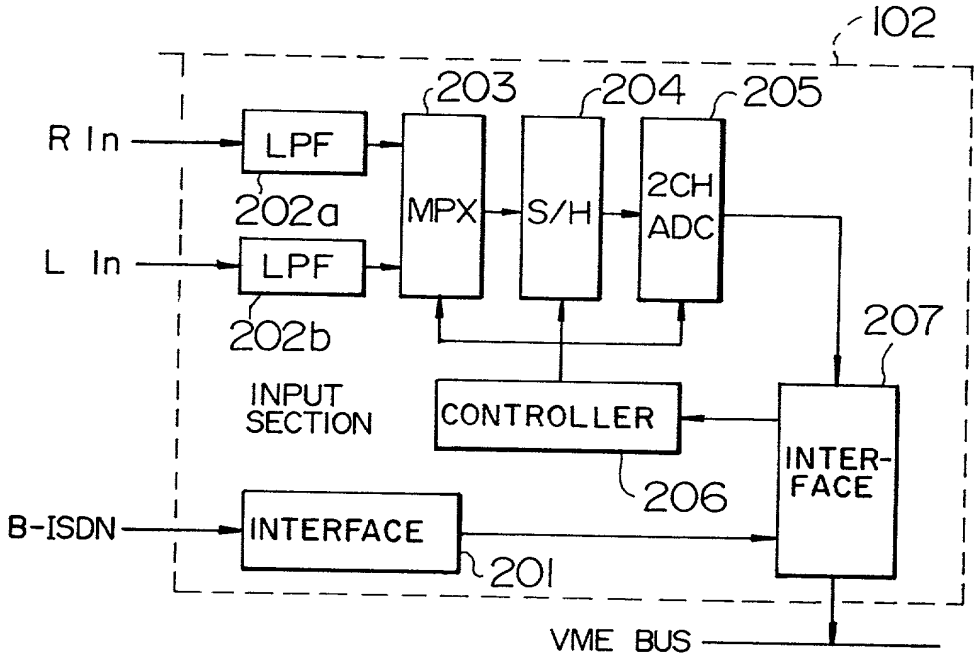
102
203
204
205
R In
LPF
202a
MPX
S/H
2CH ADC
L In
LPF
202b
207
INPUT SECTION
CONTROLLER
INTER-FACE
206
B-ISDN
INTERFACE
201
VME BUS

FIG. 3

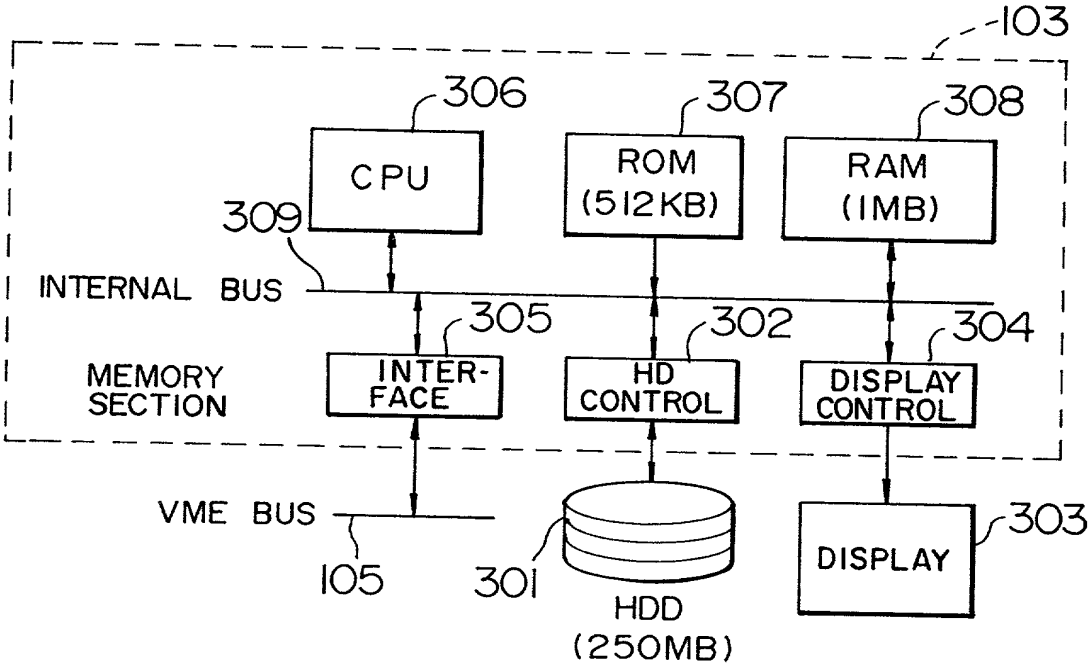
103
306
307
308
CPU
ROM (512KB)
RAM (1MB)
309
INTERNAL BUS
305
302
304
MEMORY SECTION
INTER-FACE
HD CONTROL
DISPLAY CONTROL
VME BUS
105
301
HDD (250MB)
DISPLAY
303

FIG. 4

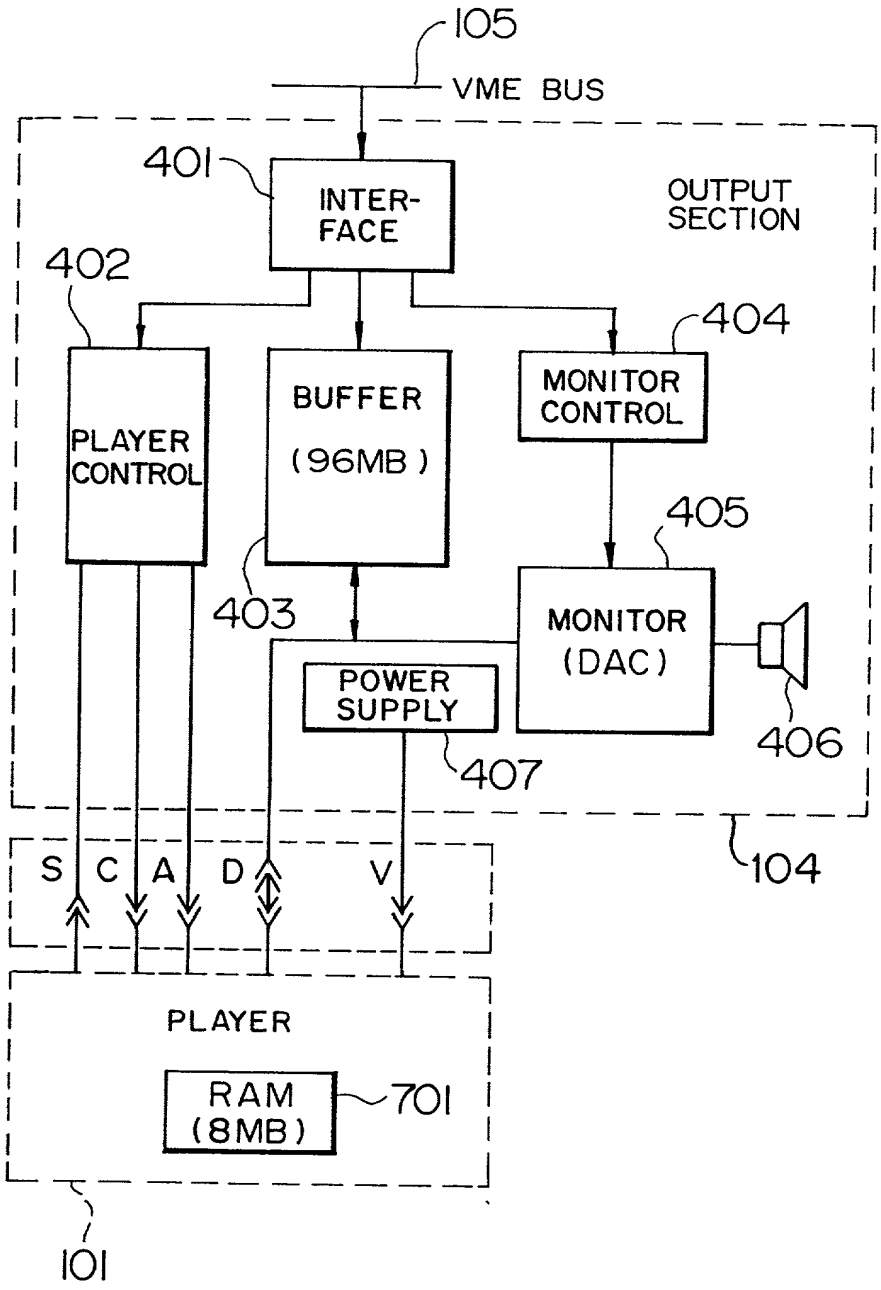
105
VME BUS
401
INTER-
FACE
OUTPUT
SECTION
402
404
PLAYER
CONTROL
BUFFER
(96MB)
MONITOR
CONTROL
405
403
MONITOR
(DAC)
POWER
SUPPLY
406
407
104
S
C
A
D
V
PLAYER
RAM
(8MB)
701
101

FIG. 5

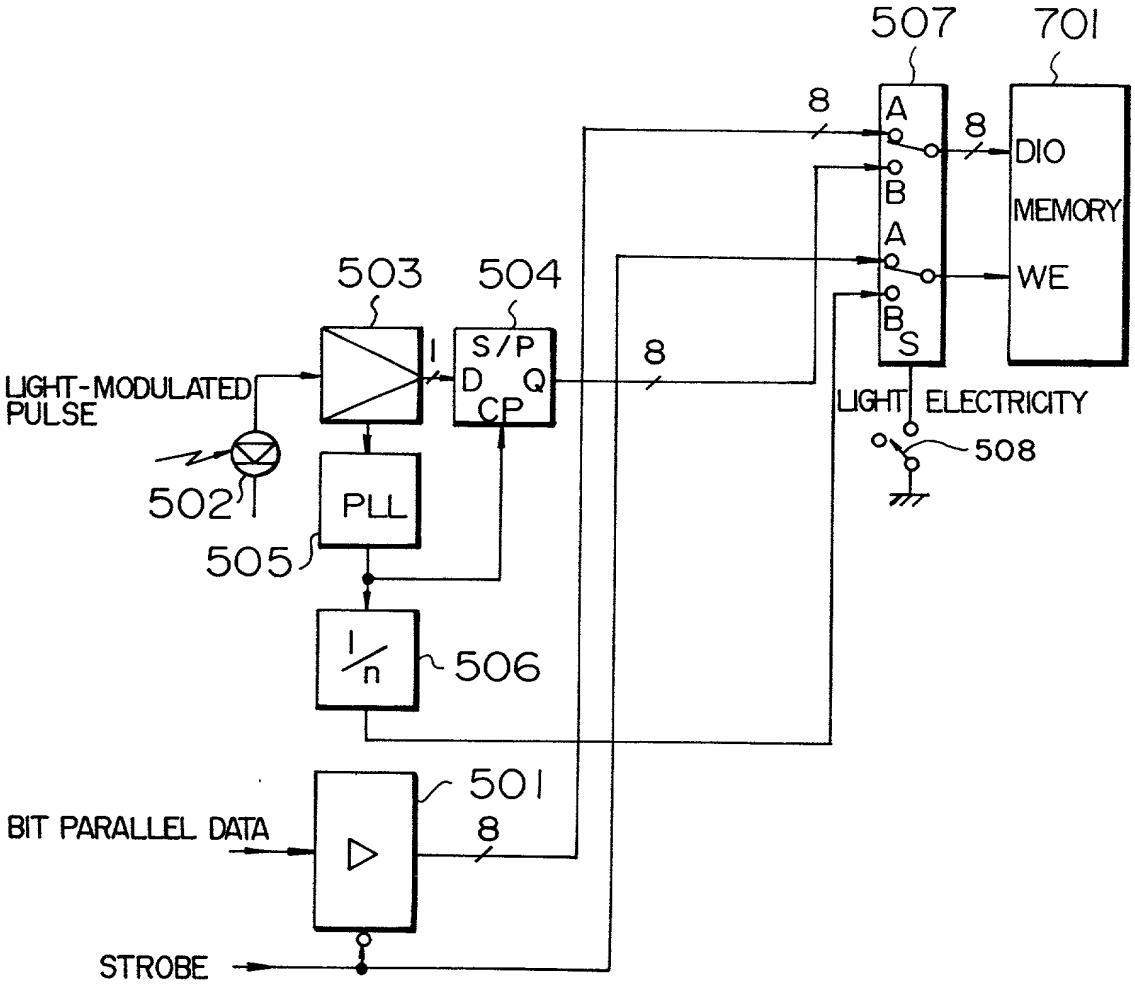
507
701
8
A
B
A
B
S
8
DIO
MEMORY
WE
503
504
S/P
D
Q
CP
1
8
LIGHT-MODULATED PULSE
LIGHT
ELECTRICITY
508
502
PLL
505
1/n
506
501
BIT PARALLEL DATA
8
STROBE

FIG. 6

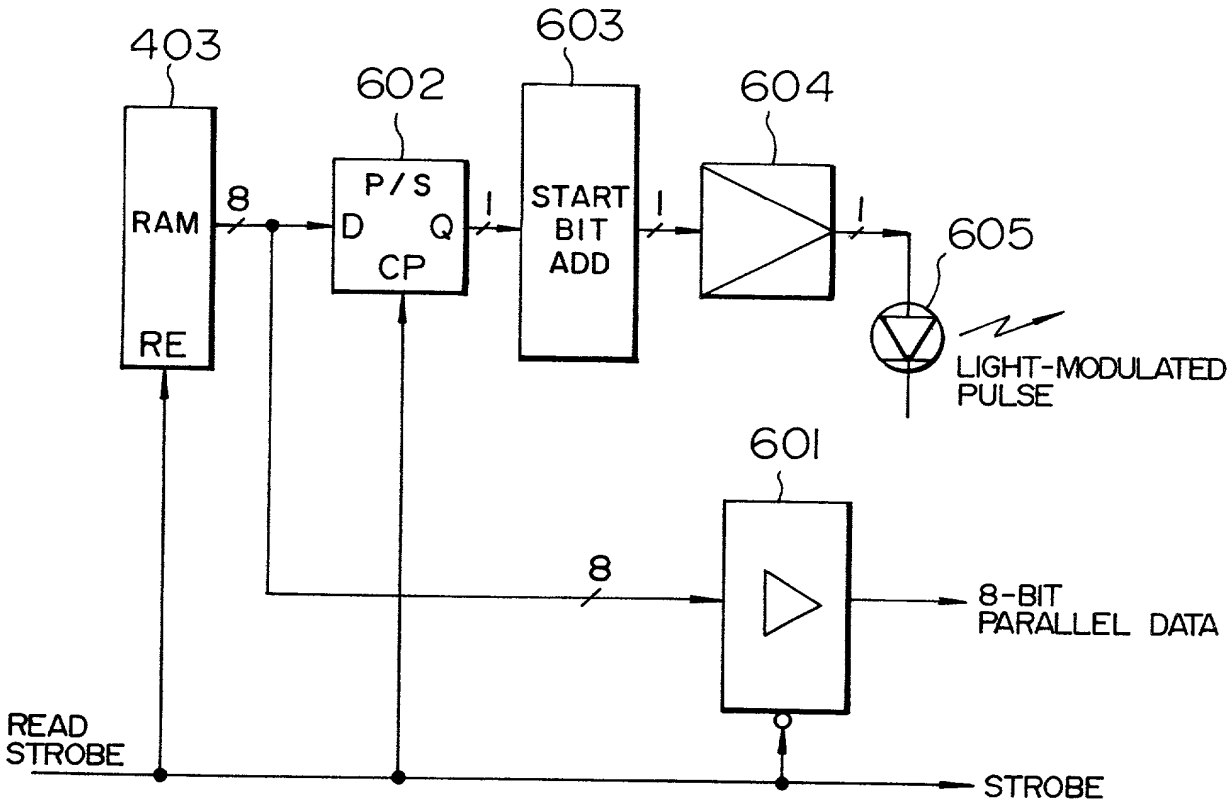
403
602
603
604
605
601
RAM
RE
8
P/S
D
Q
CP
1
START
BIT
ADD
1
1
LIGHT-MODULATED
PULSE
8
8-BIT
PARALLEL DATA
READ
STROBE
STROBE

FIG. 7

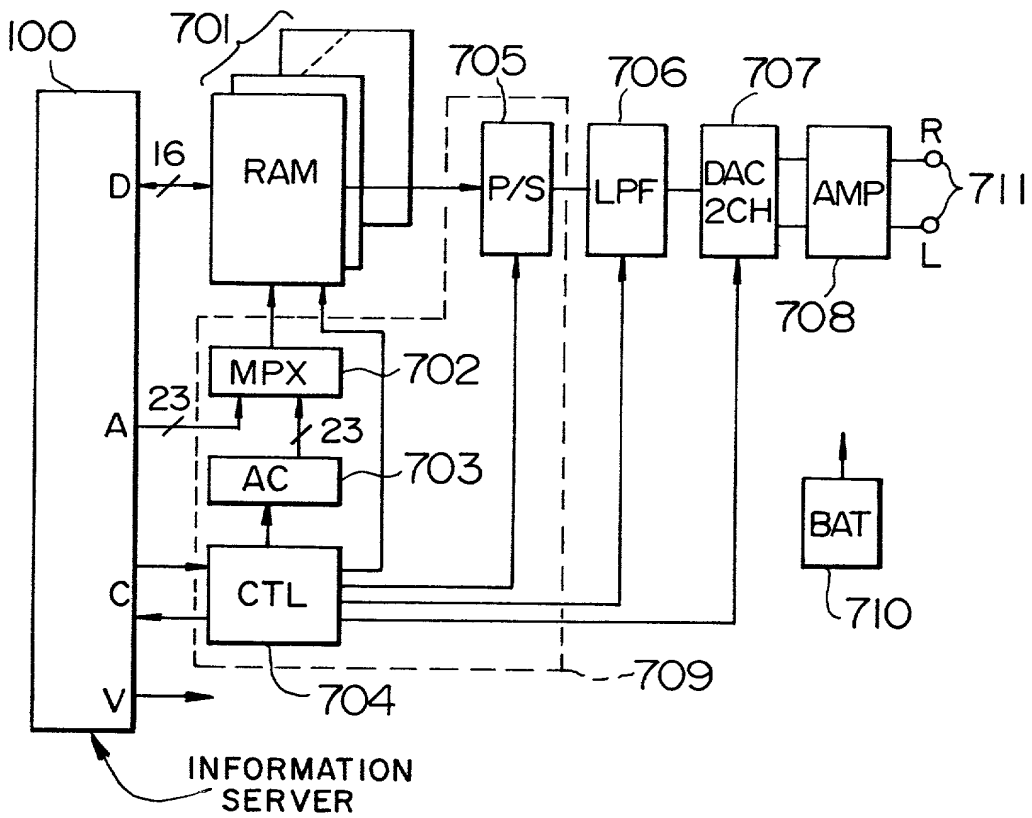
100
701
705
706
707
16
D
RAM
P/S
LPF
DAC
2CH
AMP
R
L
711
708
MPX
702
23
A
23
AC
703
BAT
710
C
CTL
709
704
V
INFORMATION
SERVER

FIG. 8

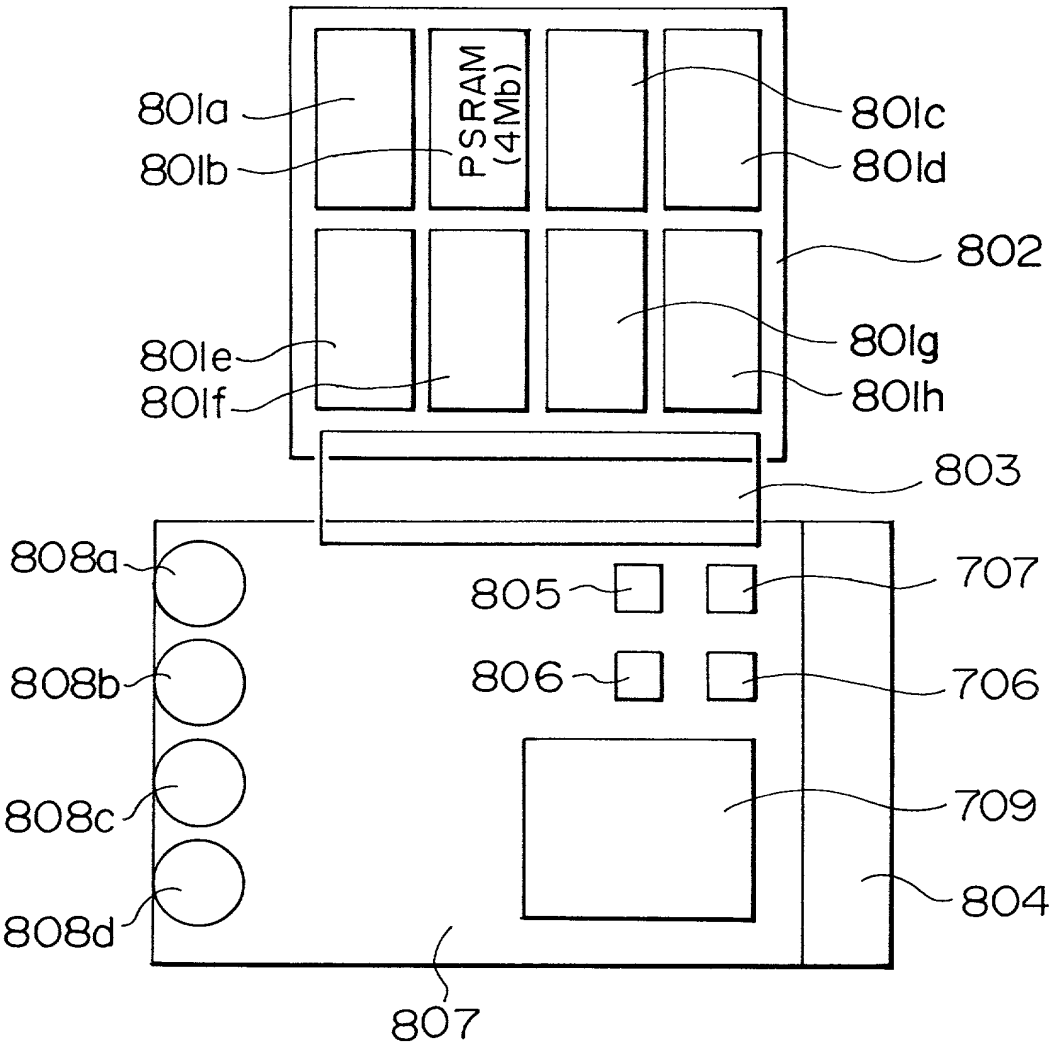
801a
801b
PSRAM (4Mb)
801c
801d
802
801e
801f
801g
801h
803
808a
808b
808c
808d
805
806
707
706
709
804
807

FIG. 9

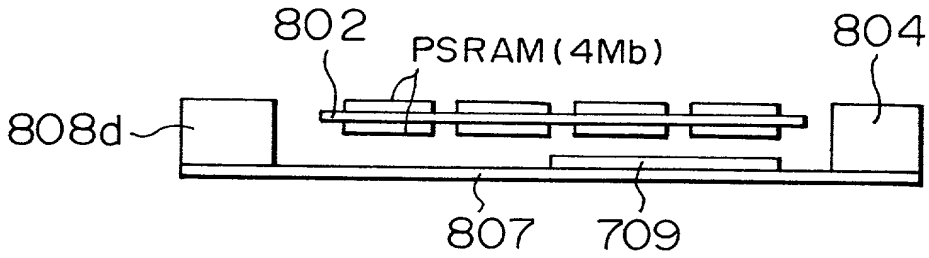
802
PSRAM (4Mb)
804
808d
807
709

FIG.10

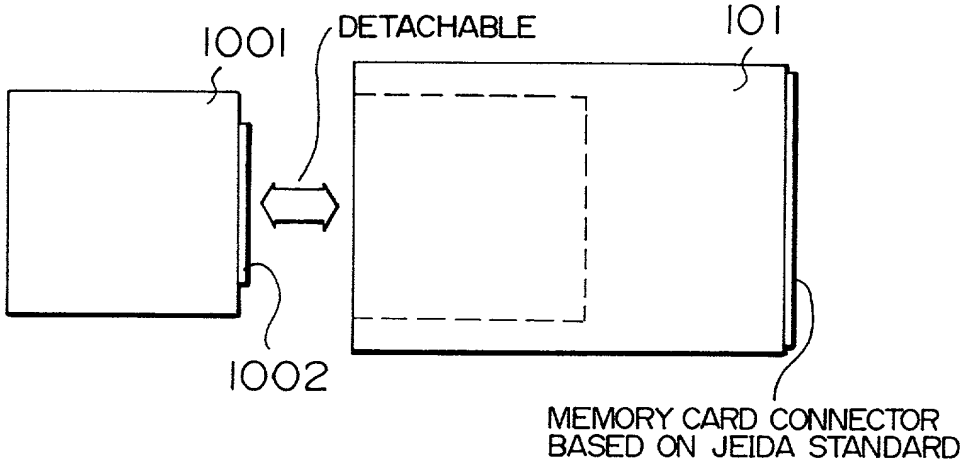
1001
DETACHABLE
101
1002
MEMORY CARD CONNECTOR
BASED ON JEIDA STANDARD

FIG.11

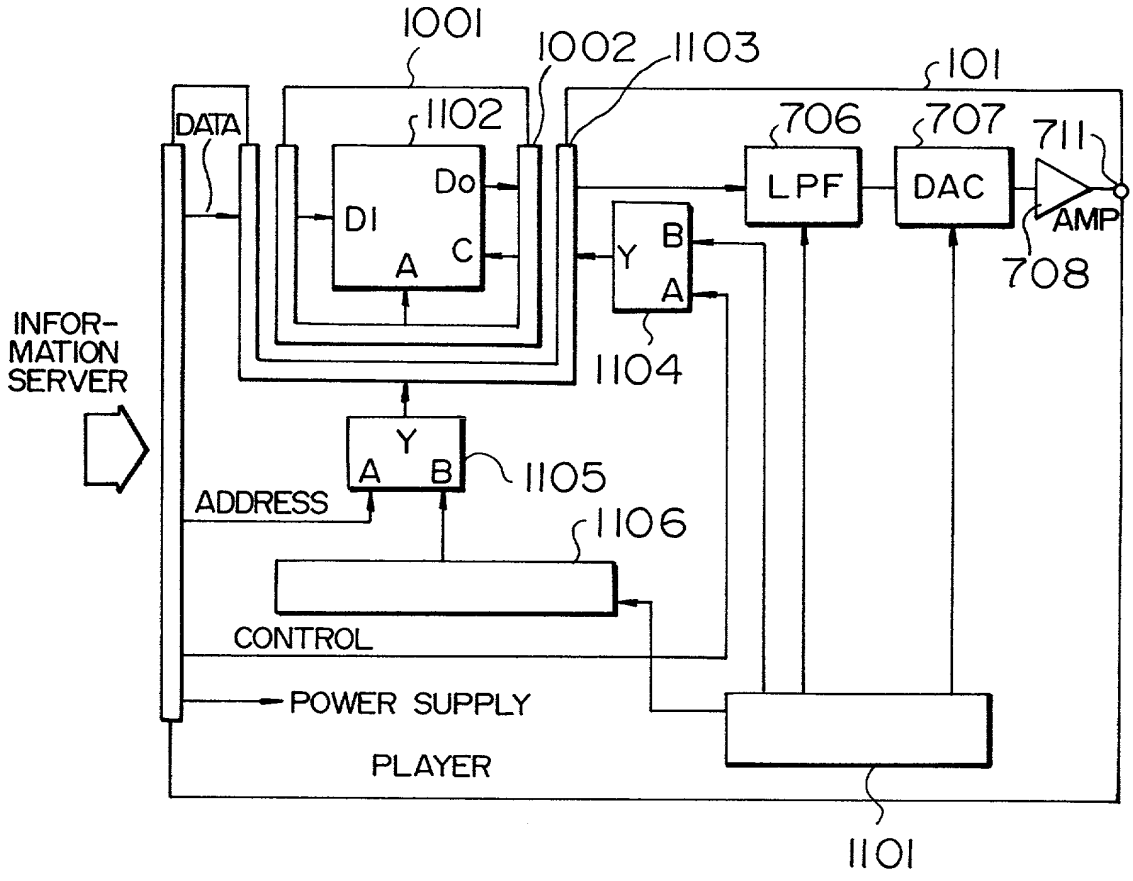
1001
1002
1103
101
DATA
1102
706
707
711
LPF
DAC
AMP
708
DI
Do
A
C
Y
B
A
1104
INFOR-
MATION
SERVER
Y
A
B
1105
ADDRESS
1106
CONTROL
POWER SUPPLY
PLAYER
1101

FIG.12

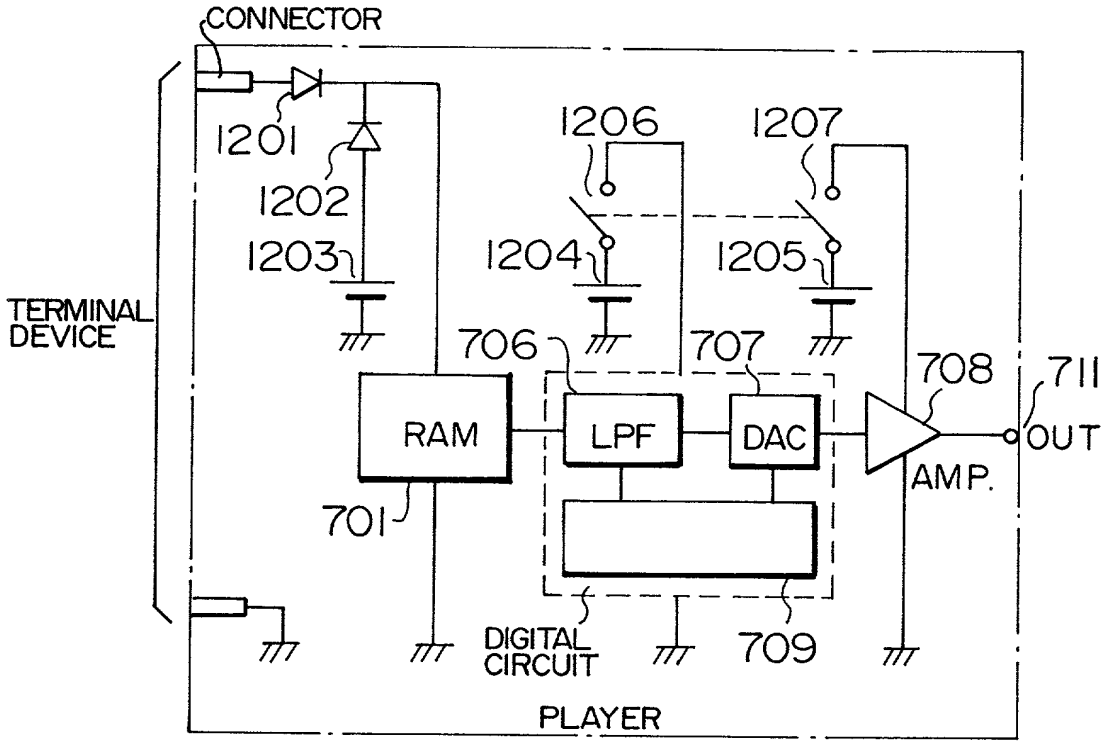
CONNECTOR
1201
1202
1203
1206
1207
1204
1205
TERMINAL DEVICE
706
707
708
711
RAM
LPF
DAC
AMP.
OUT
701
DIGITAL CIRCUIT
709
PLAYER

FIG. 13

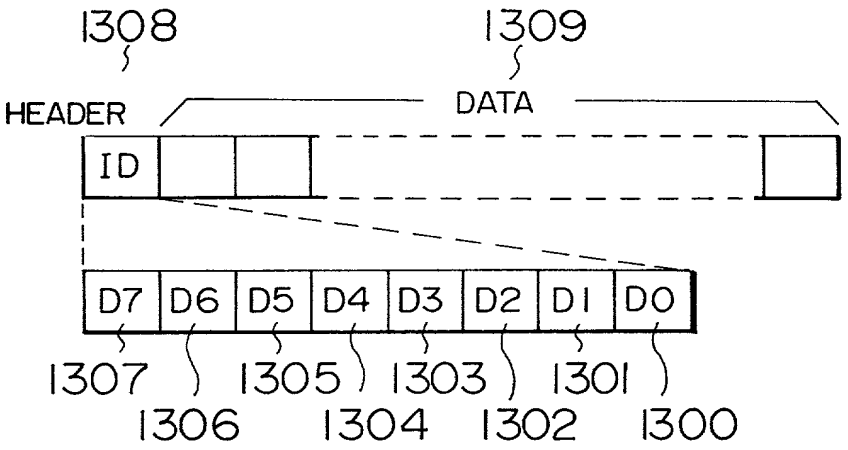
1308
1309
HEADER
DATA
ID
D7
D6
D5
D4
D3
D2
D1
D0
1307
1306
1305
1304
1303
1302
1301
1300

FIG. 14

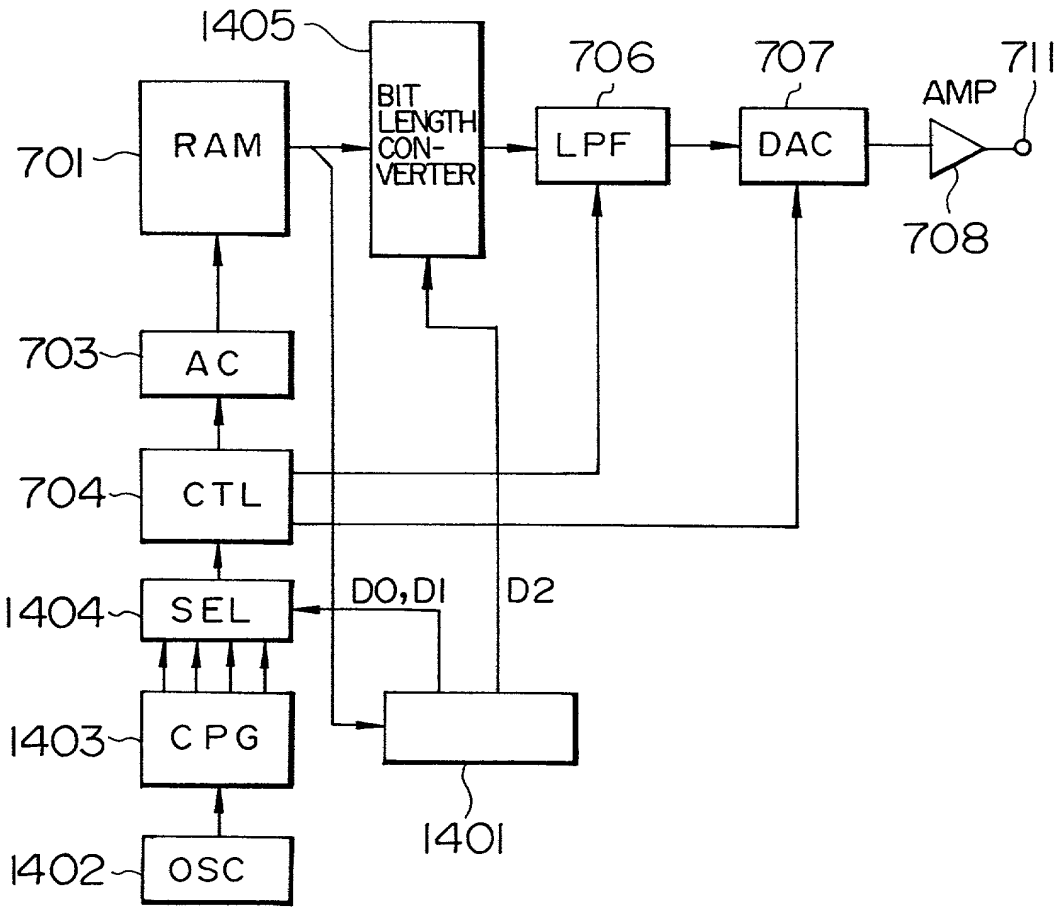
1405
BIT LENGTH CON-VERTER
706
LPF
707
DAC
711
AMP
708
701
RAM
703
AC
704
CTL
1404
SEL
DO, DI
D2
1403
CPG
1402
OSC
1401

FIG.15

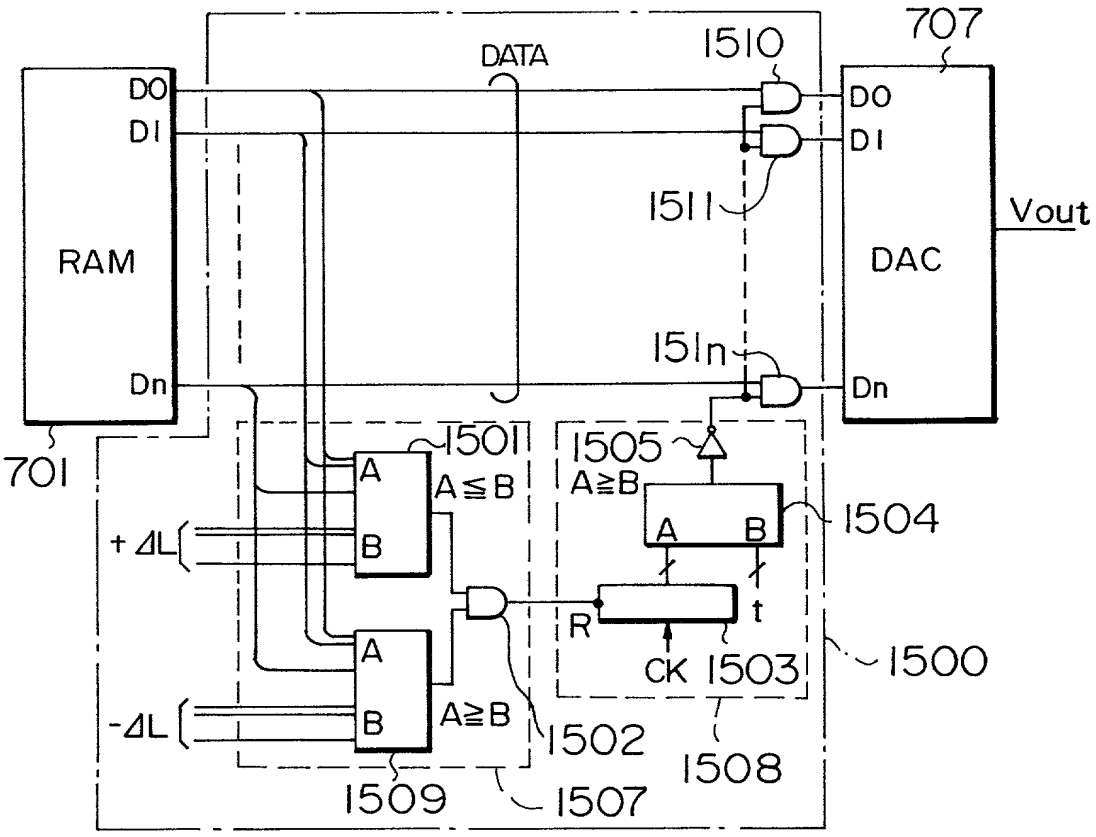
DATA
1510
707
D0
D1
RAM
Dn
701
1511
Vout
DAC
151n
1501
1505
A≧B
A≦B
A
B
+ΔL
-ΔL
1504
t
R
CK
1503
1500
1502
1508
1509
1507

FIG.16

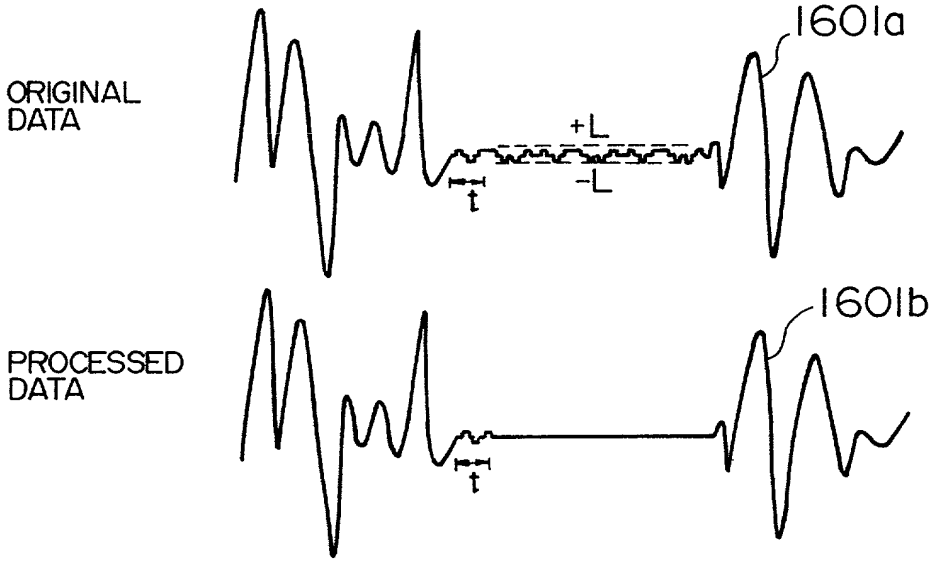
ORIGINAL DATA
1601a
+L
-L
t
PROCESSED DATA
1601b
t

FIG.17

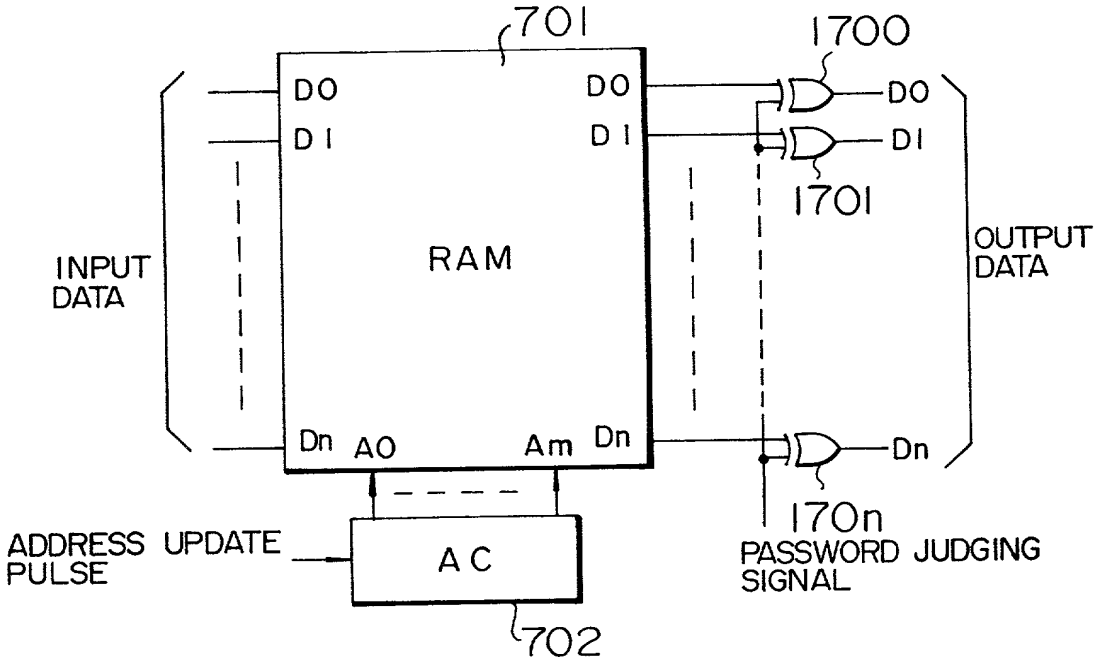
701
1700
DO
DI
DO
DI
DO
DI
1701
INPUT DATA
RAM
OUTPUT DATA
Dn
A0
Am
Dn
Dn
170n
ADDRESS UPDATE PULSE
AC
PASSWORD JUDGING SIGNAL
702

FIG.18

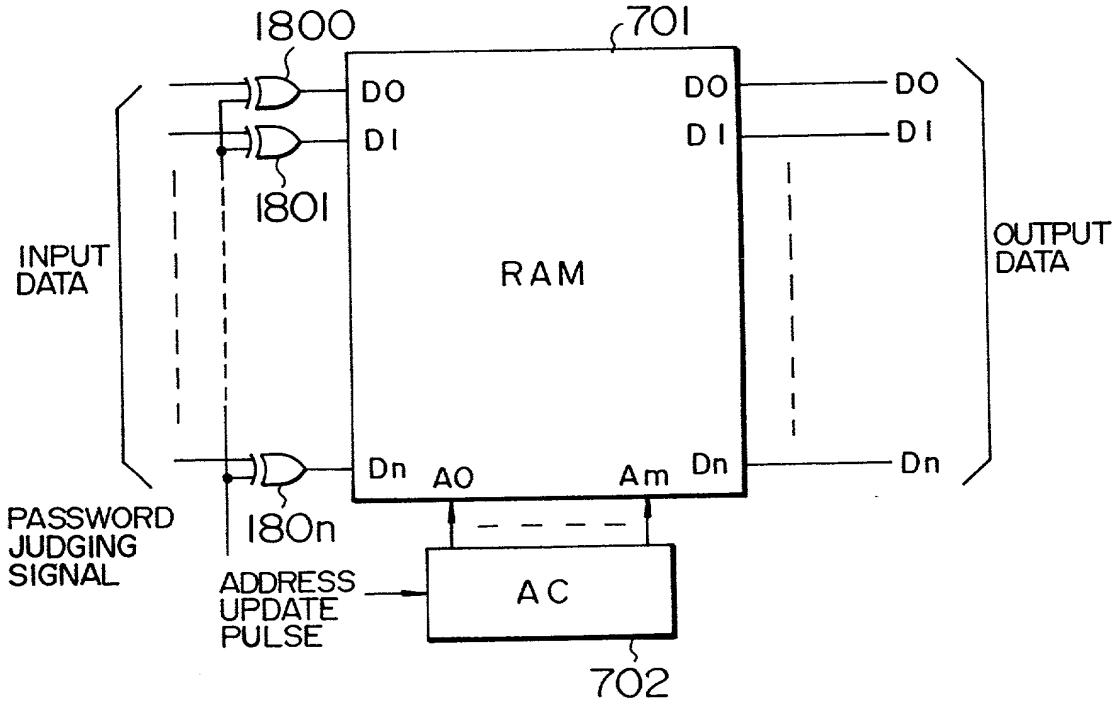
1800
701
DO
DI
DO
DI
DO
DI
1801
INPUT DATA
RAM
OUTPUT DATA
Dn
A0
Am
Dn
Dn
PASSWORD JUDGING SIGNAL
180n
ADDRESS UPDATE PULSE
AC
702

FIG.19

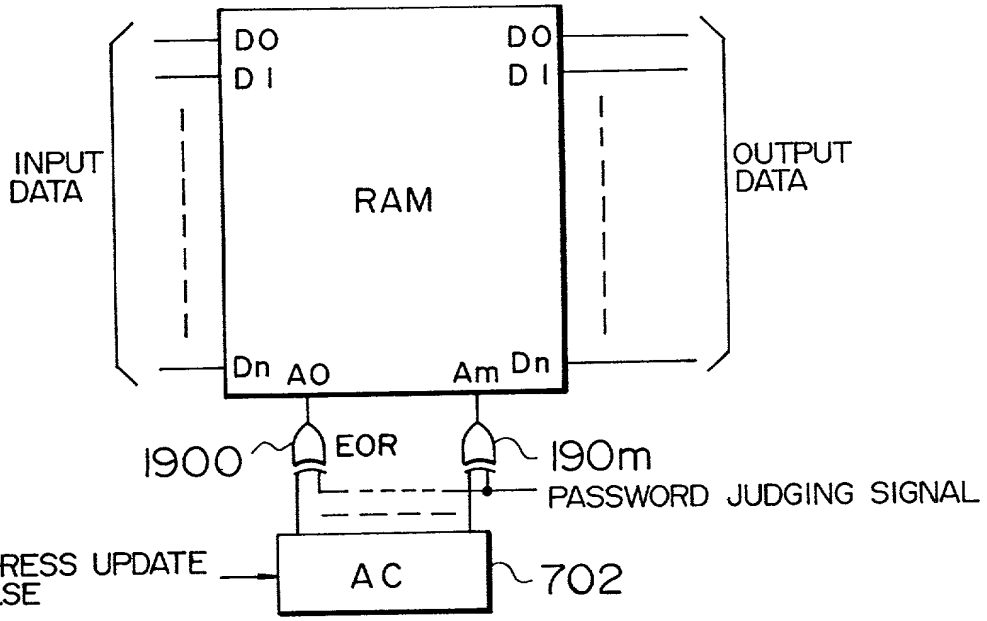
DO
DI
DO
DI
INPUT DATA
RAM
OUTPUT DATA
Dn AO
Am Dn
1900
EOR
190m
PASSWORD JUDGING SIGNAL
ADDRESS UPDATE PULSE
AC
702

FIG. 20

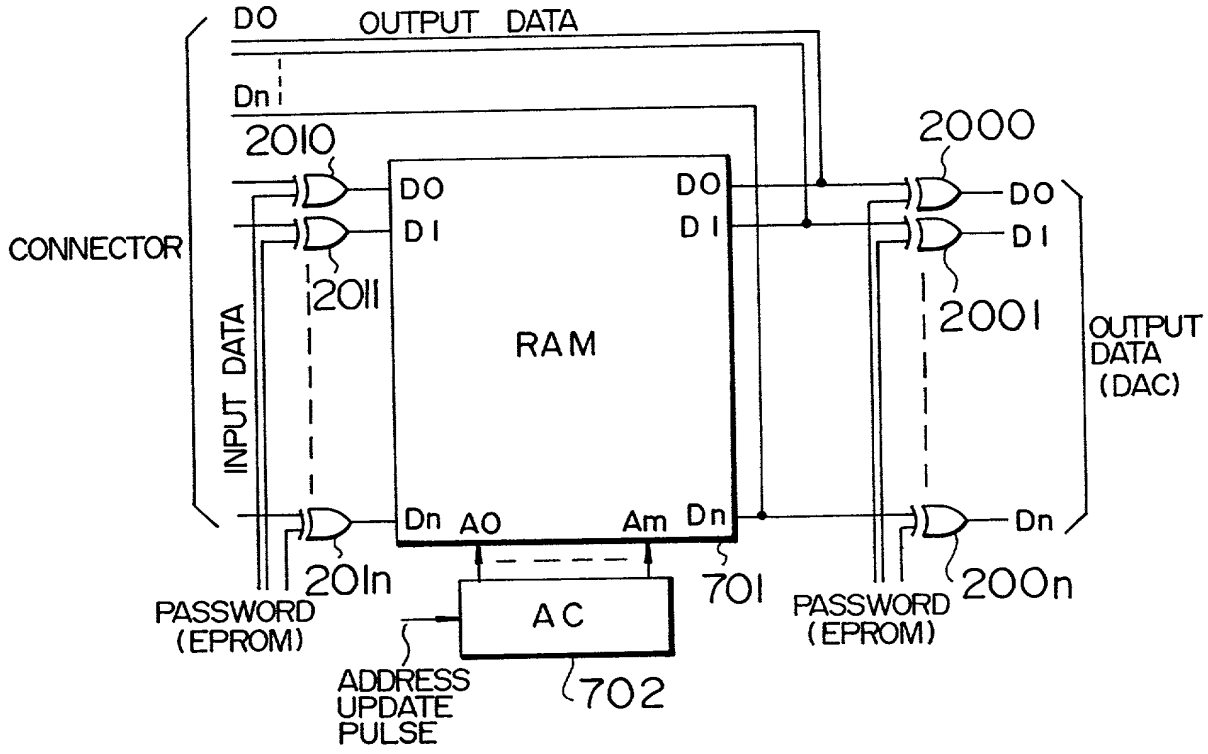
DO
OUTPUT DATA
Dn
2010
2000
DO
DI
DO
DI
CONNECTOR
2011
2001
INPUT DATA
RAM
OUTPUT DATA (DAC)
Dn AO
Am Dn
Dn
201n
701
200n
PASSWORD (EPROM)
AC
PASSWORD (EPROM)
ADDRESS UPDATE PULSE
702

FIG. 21

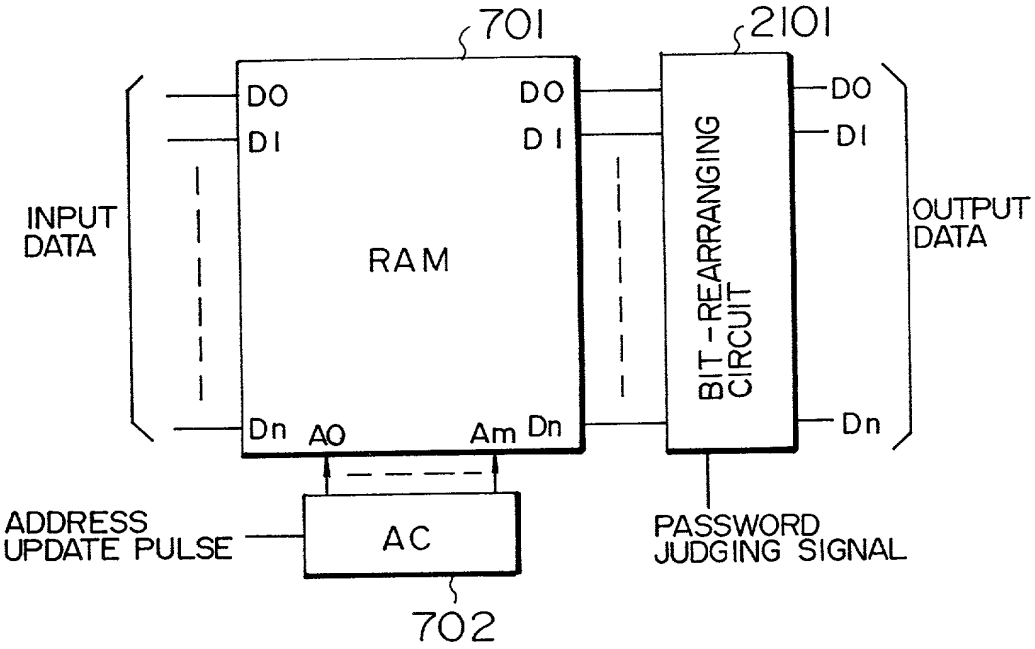
701
2101
DO
DI
Dn
AO
Am
RAM
BIT-REARRANGING CIRCUIT
INPUT DATA
OUTPUT DATA
ADDRESS UPDATE PULSE
AC
PASSWORD JUDGING SIGNAL
702

FIG. 22

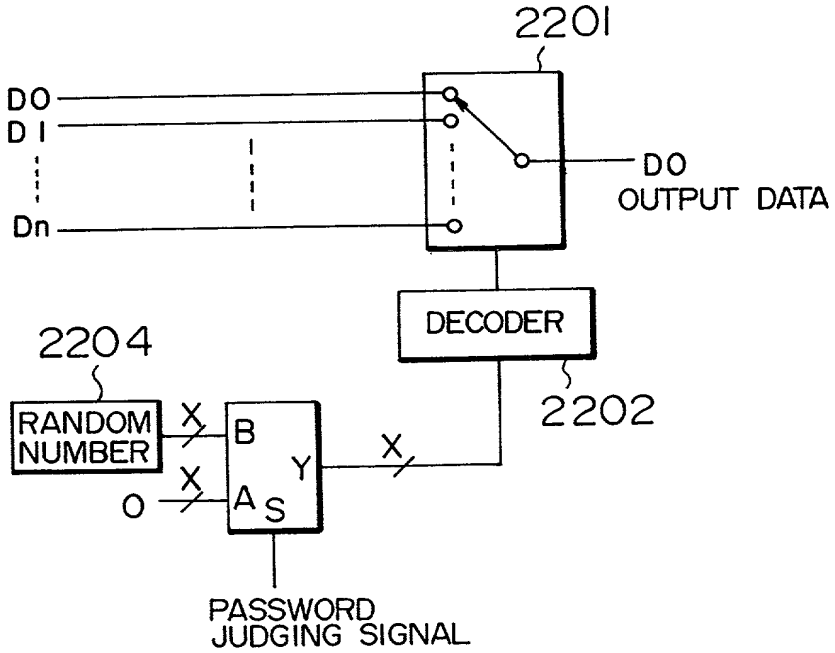
2201
DO
DI
Dn
DO
OUTPUT DATA
DECODER
2204
2202
RANDOM NUMBER
X
B
Y
A
S
0
PASSWORD JUDGING SIGNAL

FIG. 23

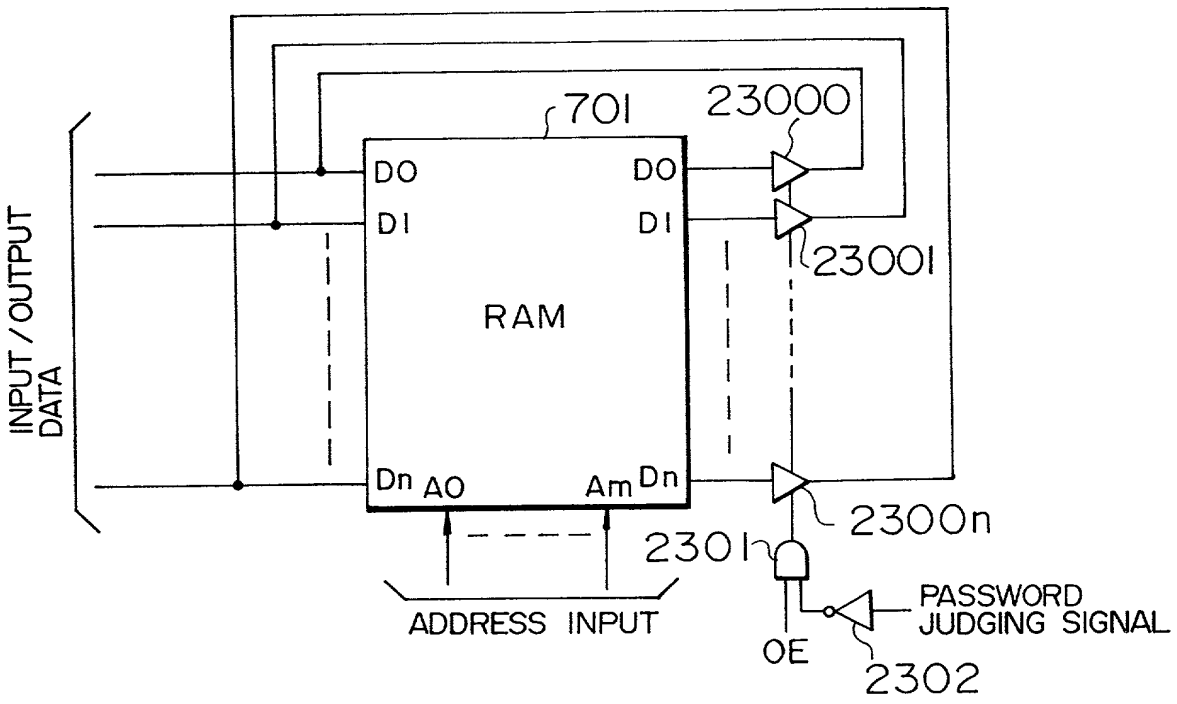
701
23000
DO
DO
DI
DI
23001
RAM
INPUT / OUTPUT DATA
Dn AO
Am Dn
2300n
2301n
PASSWORD JUDGING SIGNAL
ADDRESS INPUT
OE
2302

FIG. 24

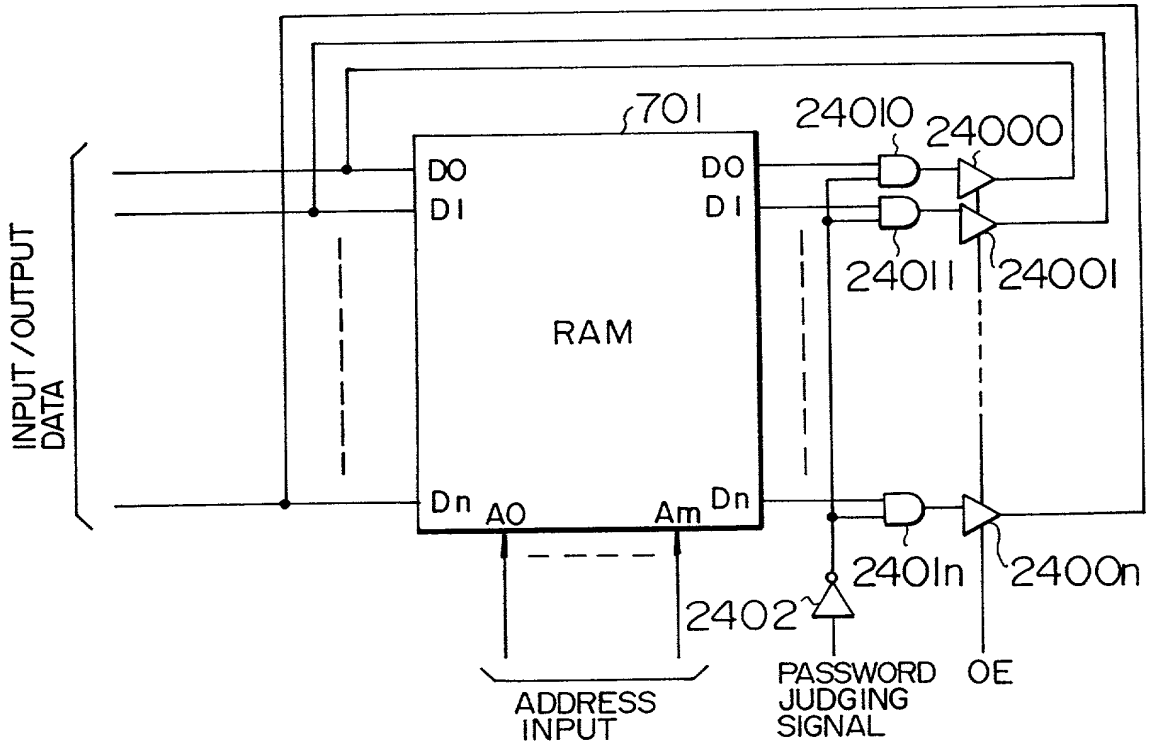
701
24010
24000
DO
DO
DI
DI
24011
24001
RAM
INPUT / OUTPUT DATA
Dn AO
Am Dn
2401n
2400n
2402
ADDRESS INPUT
PASSWORD JUDGING SIGNAL
OE

FIG. 25

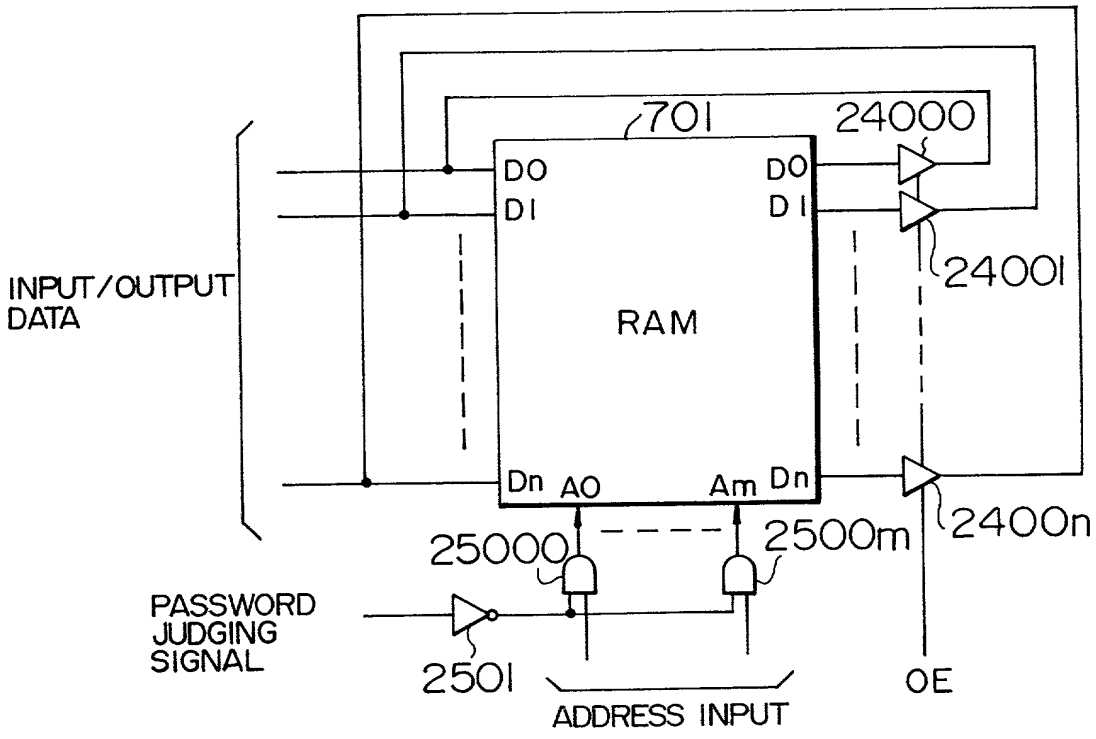
701
24000
DO
DI
DO
DI
24001
INPUT/OUTPUT
DATA
RAM
Dn
AO
Am
Dn
2400n
25000
2500m
PASSWORD
JUDGING
SIGNAL
2501
ADDRESS INPUT
OE

FIG. 26

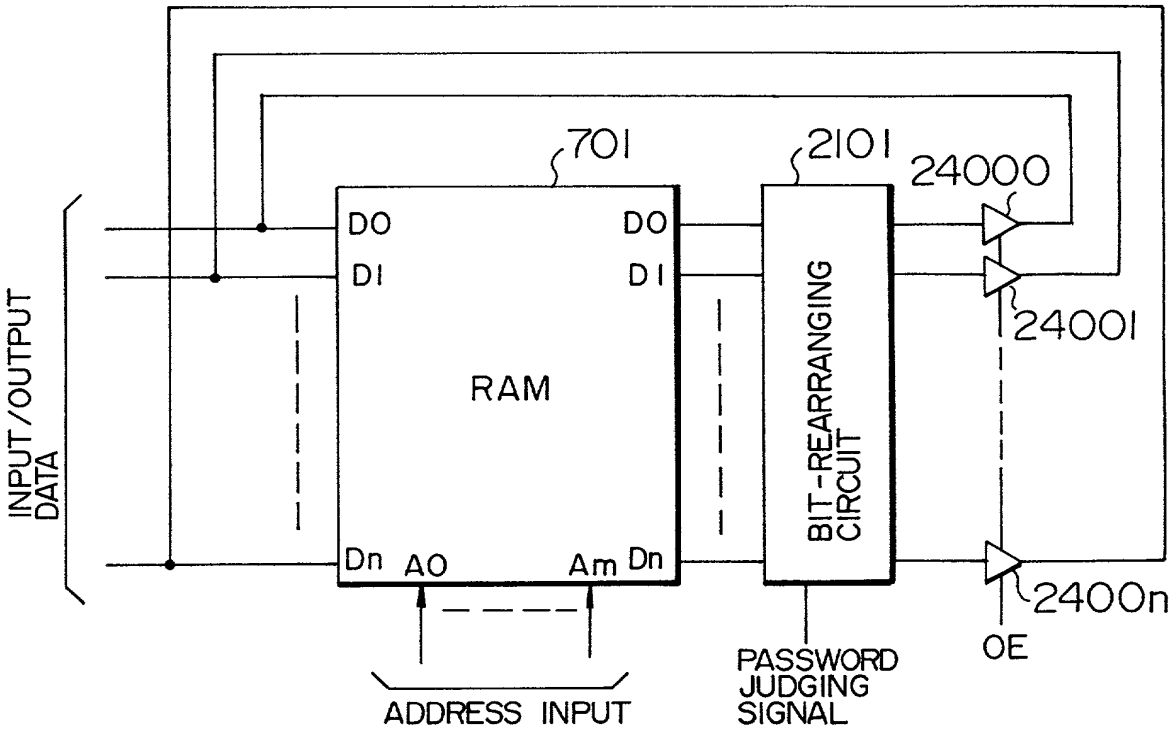
701
2101
24000
24001
2400n
DO
DI
Dn
A0
Am
RAM
BIT-REARRANGING CIRCUIT
INPUT/OUTPUT DATA
ADDRESS INPUT
PASSWORD JUDGING SIGNAL
OE

FIG. 27

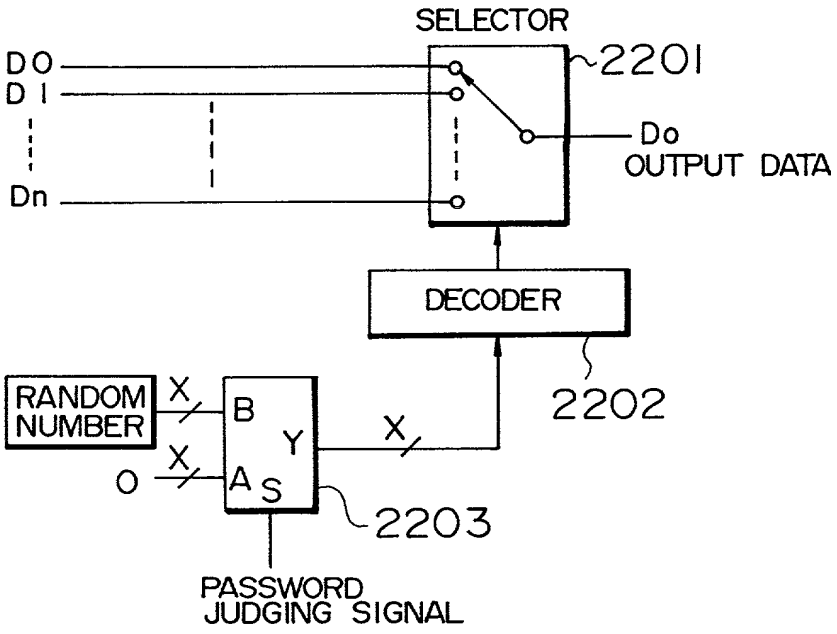
SELECTOR
2201
DO
DI
Dn
Do
OUTPUT DATA
DECODER
2202
RANDOM NUMBER
X
B
Y
X
0
X
A
S
2203
PASSWORD JUDGING SIGNAL

FIG. 28

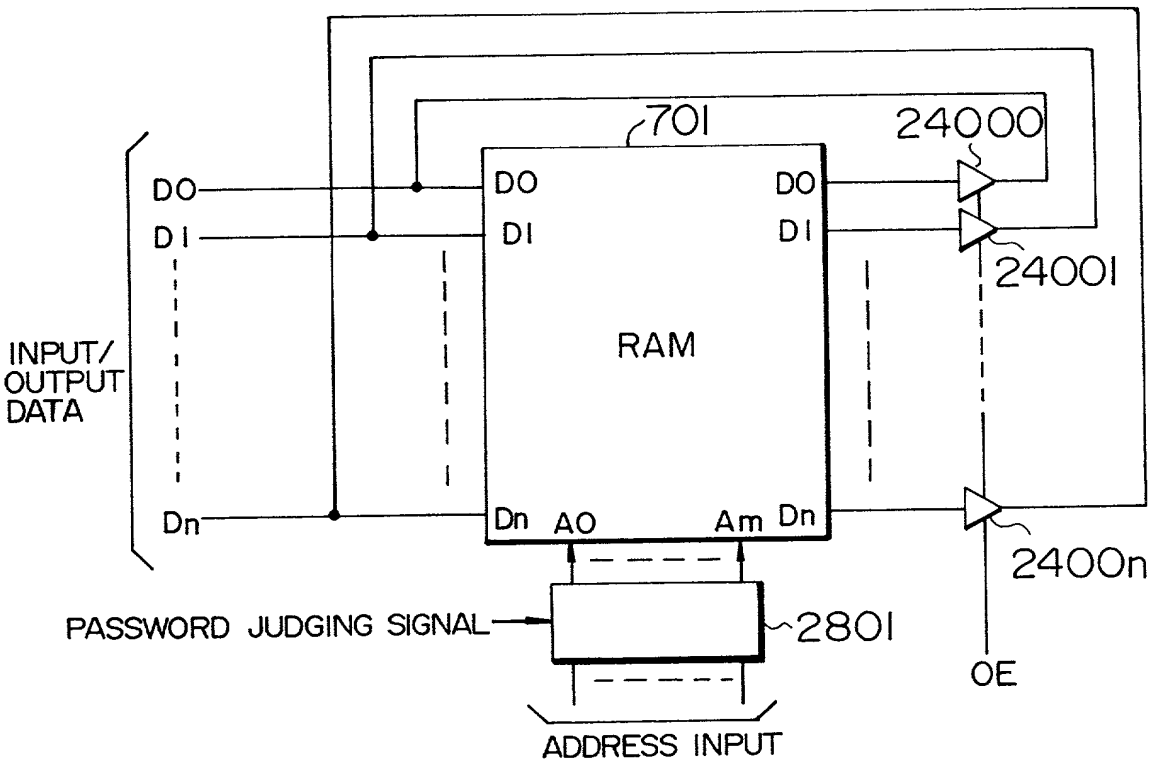
701
24000
DO
DI
Dn
INPUT/
OUTPUT
DATA
RAM
24001
2400n
A0
Am
PASSWORD JUDGING SIGNAL
2801
OE
ADDRESS INPUT

FIG. 29

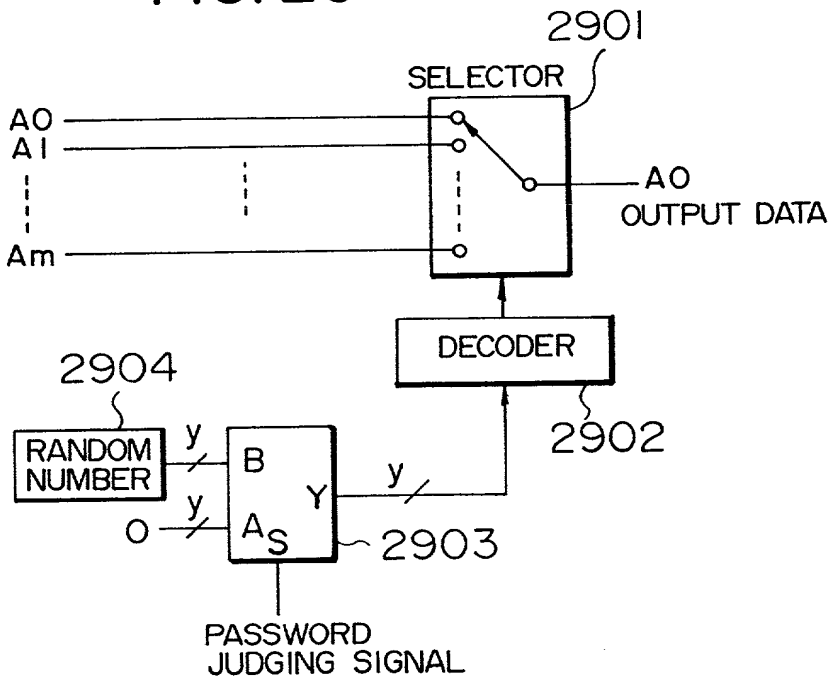
2901
SELECTOR
A0
A1
Am
A0
OUTPUT DATA
DECODER
2902
2904
RANDOM
NUMBER
y
B
Y
0
As
2903
PASSWORD
JUDGING SIGNAL

FIG. 30

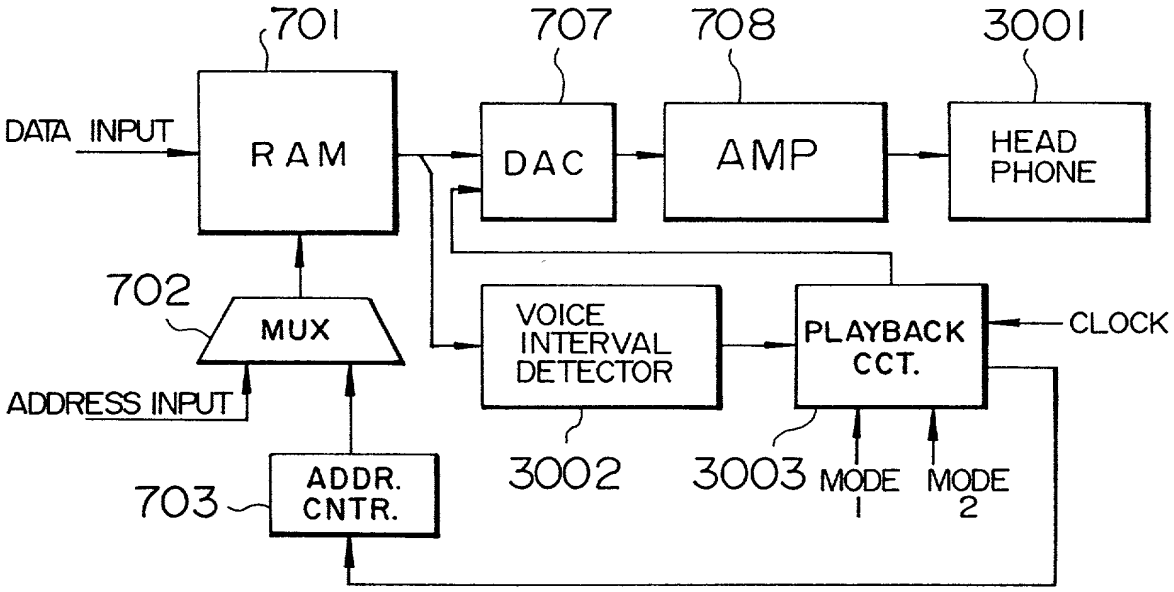
701
707
708
3001
DATA INPUT
RAM
DAC
AMP
HEAD PHONE
702
MUX
VOICE INTERVAL DETECTOR
PLAYBACK CCT.
CLOCK
ADDRESS INPUT
703
ADDR. CNTR.
3002
3003
MODE 1
MODE 2

FIG. 31

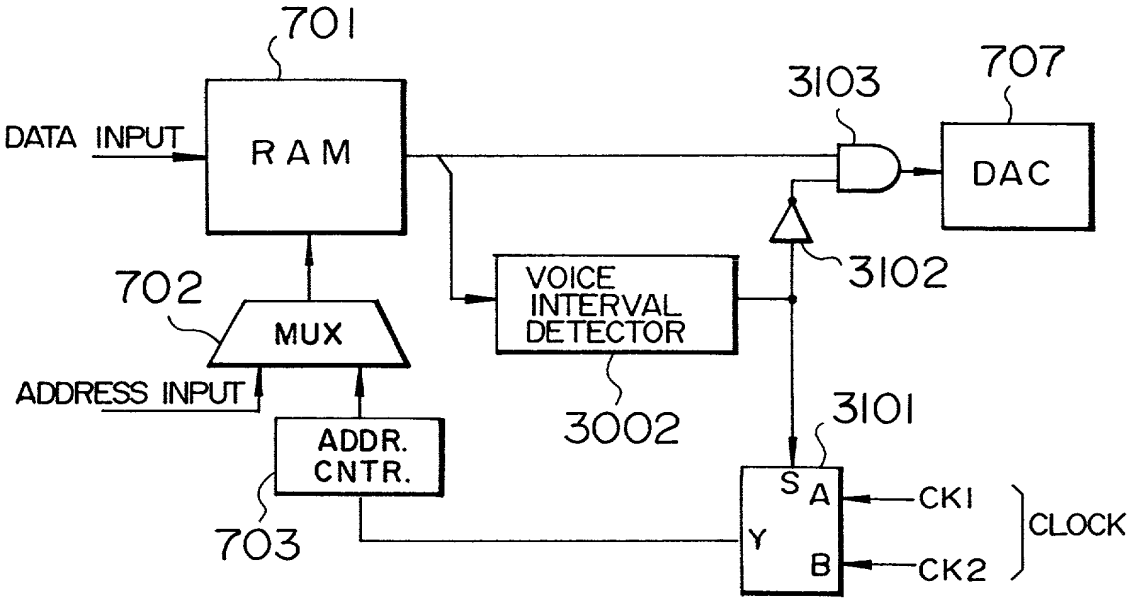
701
3103
707
DATA INPUT
RAM
DAC
3102
702
MUX
VOICE INTERVAL DETECTOR
ADDRESS INPUT
3002
3101
ADDR. CNTR.
703
S
A
CK1
CLOCK
Y
B
CK2

FIG. 32

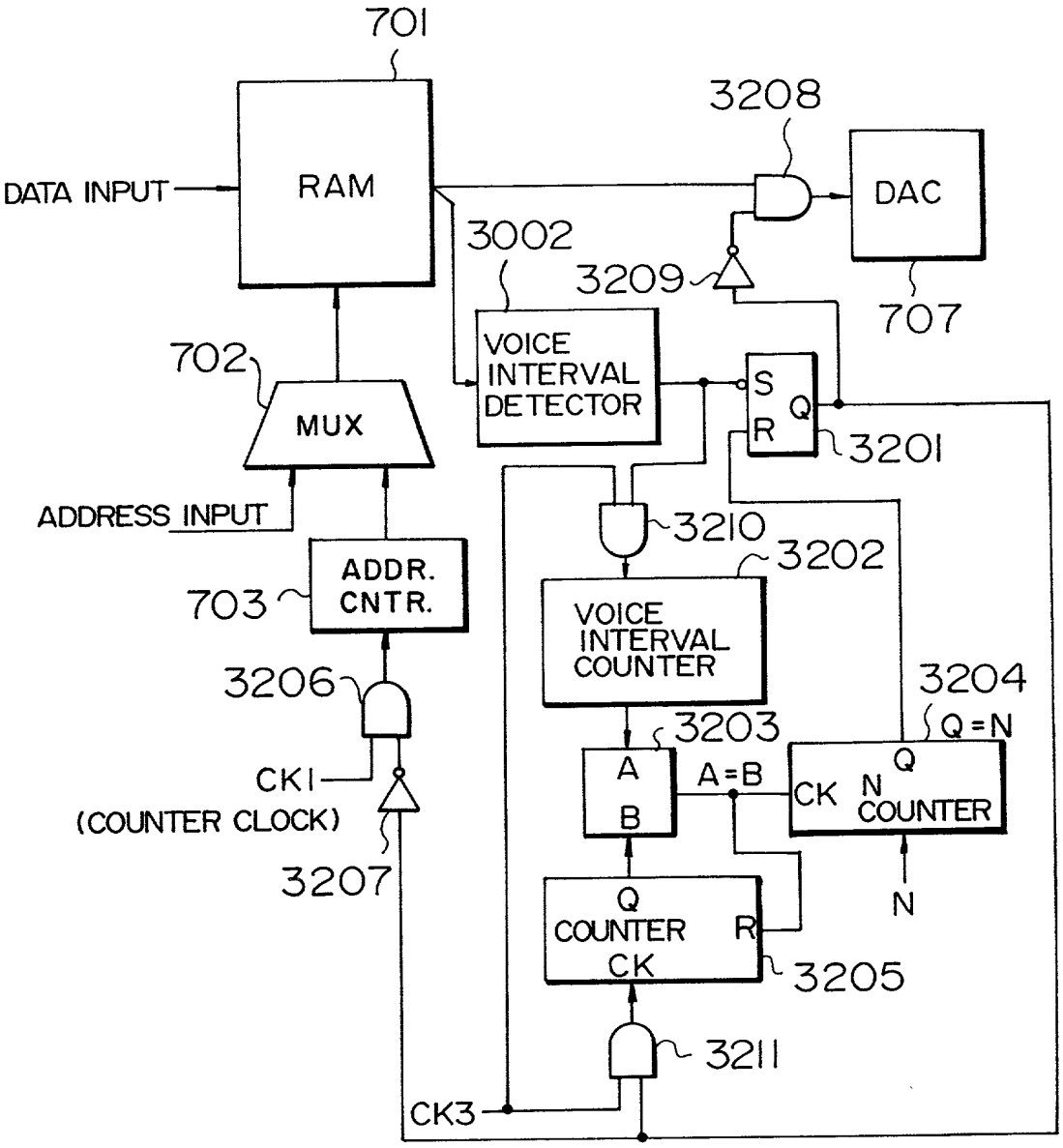
701
RAM
DATA INPUT
3208
DAC
707
3002
3209
VOICE
INTERVAL
DETECTOR
S
R
Q
3201
702
MUX
ADDRESS INPUT
3210
3202
703
ADDR.
CNTR.
VOICE
INTERVAL
COUNTER
3204
Q=N
3206
3203
A
B
A=B
CK
N
COUNTER
Q
CK1
(COUNTER CLOCK)
3207
Q
COUNTER
CK
R
3205
N
3211
CK3

FIG. 33

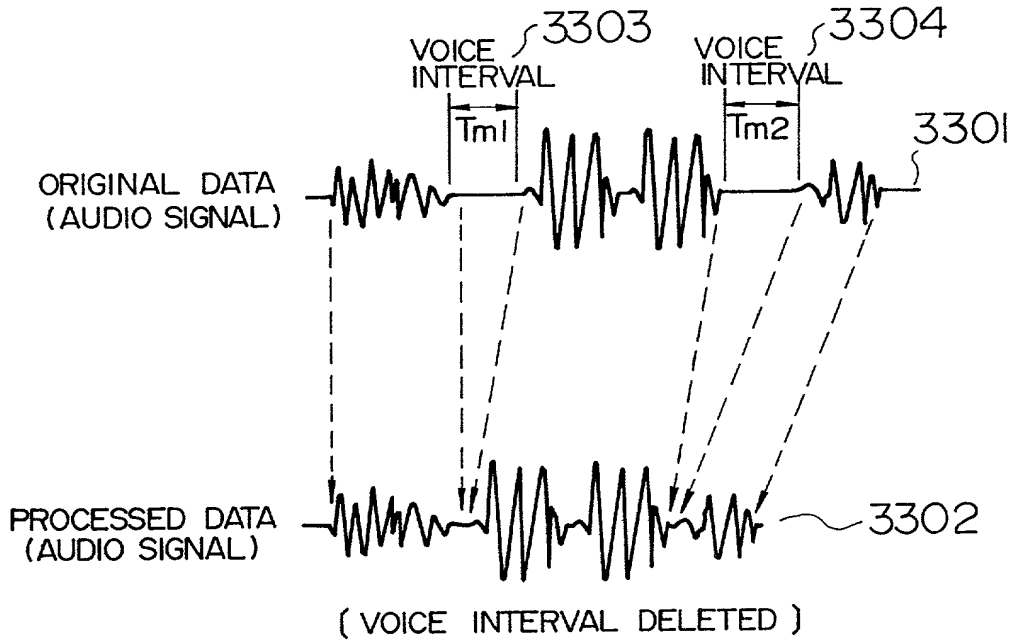
VOICE INTERVAL
3303
VOICE INTERVAL
3304
Tm1
Tm2
3301
ORIGINAL DATA (AUDIO SIGNAL)
PROCESSED DATA (AUDIO SIGNAL)
3302
(VOICE INTERVAL DELETED)

FIG. 34

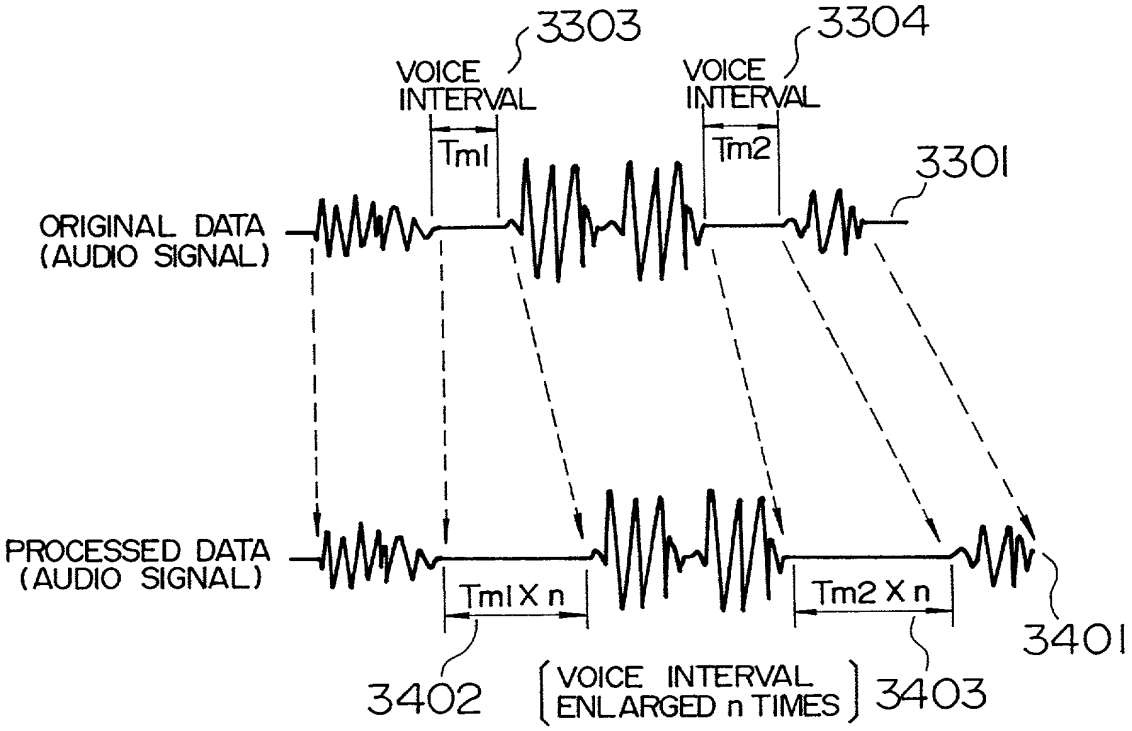
3303
VOICE INTERVAL
3304
VOICE INTERVAL
Tm1
Tm2
3301
ORIGINAL DATA (AUDIO SIGNAL)
PROCESSED DATA (AUDIO SIGNAL)
Tm1 X n
Tm2 X n
3401
3402
VOICE INTERVAL ENLARGED n TIMES
3403

FIG. 35

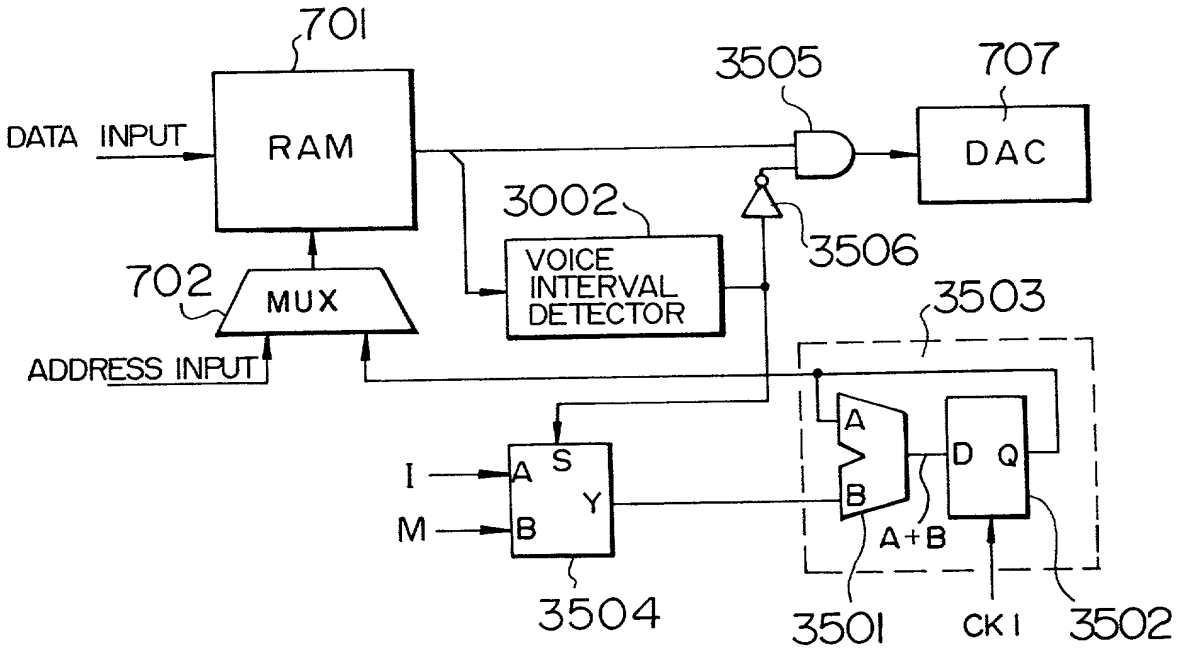
701
3505
707
DATA INPUT
RAM
DAC
3002
3506
VOICE
INTERVAL
DETECTOR
702
MUX
3503
ADDRESS INPUT
A
S
D Q
I
A
Y
B
M
B
A+B
3504
3501
CK1
3502

FIG. 36

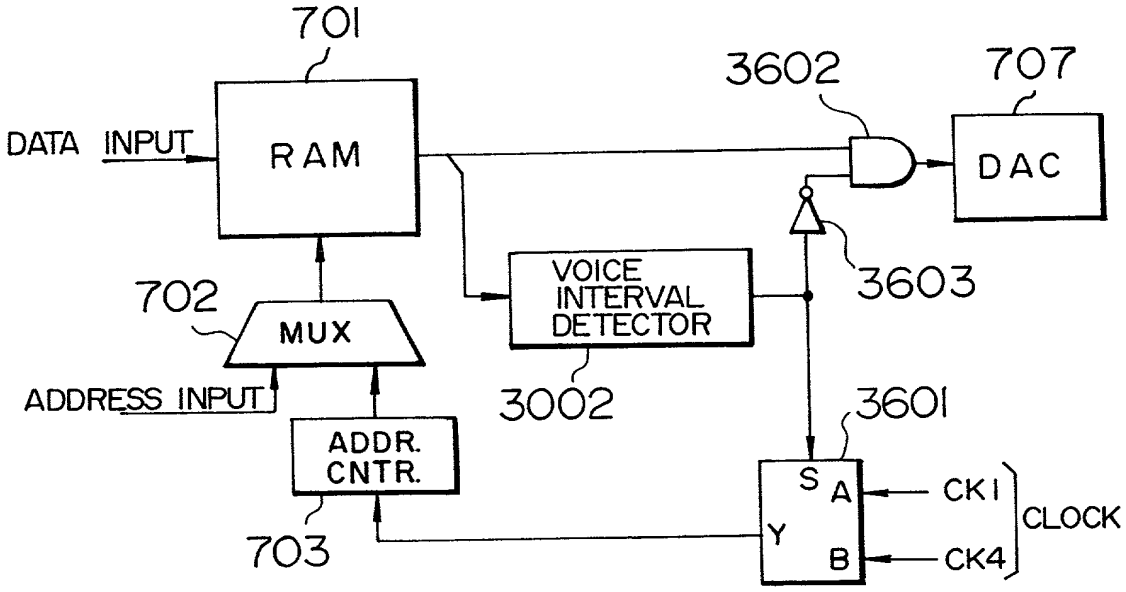
701
3602
707
DATA INPUT
RAM
DAC
3603
VOICE
INTERVAL
DETECTOR
702
MUX
ADDRESS INPUT
3002
3601
ADDR.
CNTR.
S
A
CK1
CLOCK
Y
B
CK4
703

FIG.37

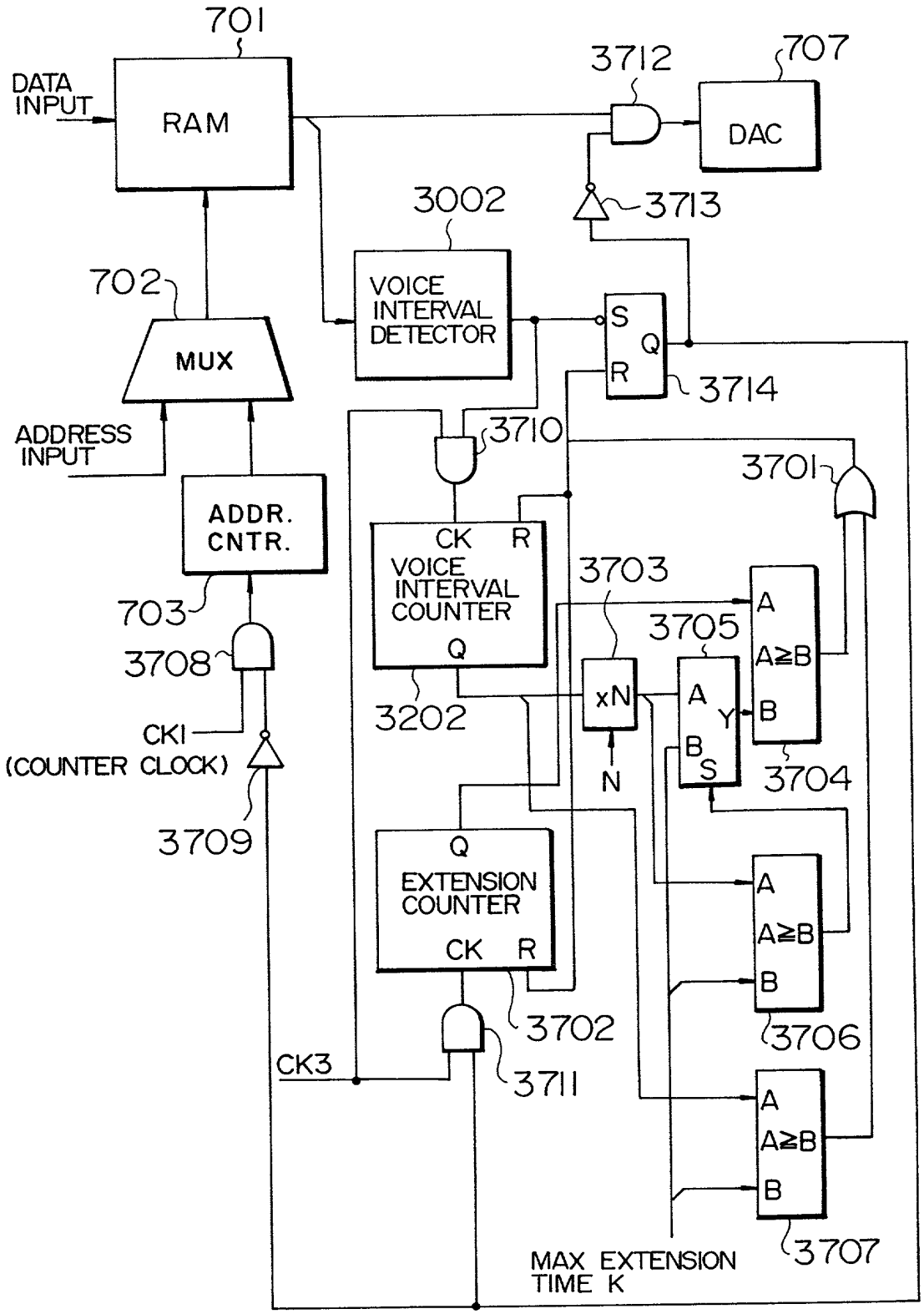
701
DATA INPUT
RAM
3712
707
DAC
3713
3002
VOICE INTERVAL DETECTOR
S
Q
R
3714
702
MUX
ADDRESS INPUT
3710
3701
ADDR. CNTR.
CK R
VOICE INTERVAL COUNTER
Q
3703
3705
A
A≥B
B
703
3708
xN
A
Y
B
S
3704
3202
CKI
(COUNTER CLOCK)
N
3709
Q
EXTENSION COUNTER
CK R
A
A≥B
B
3706
3702
CK3
3711
A
A≥B
B
3707
MAX EXTENSION TIME K

FIG. 38

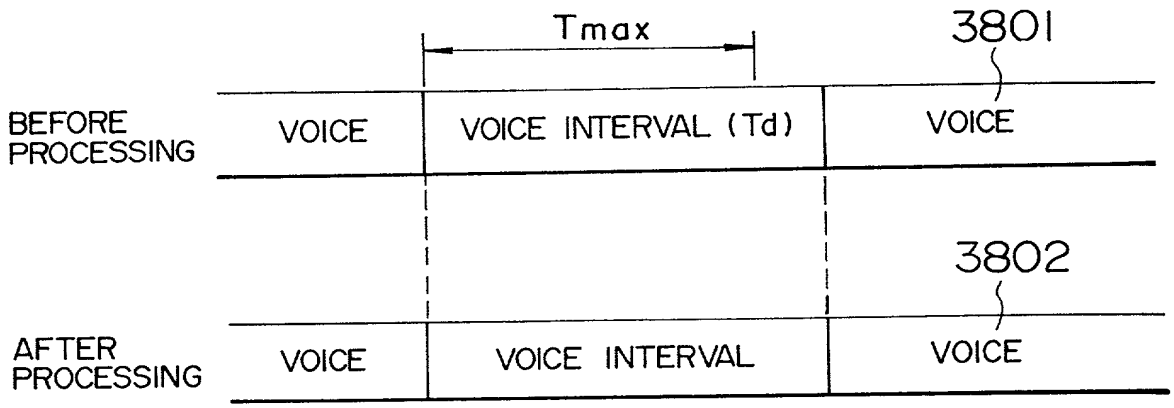

FIG. 39

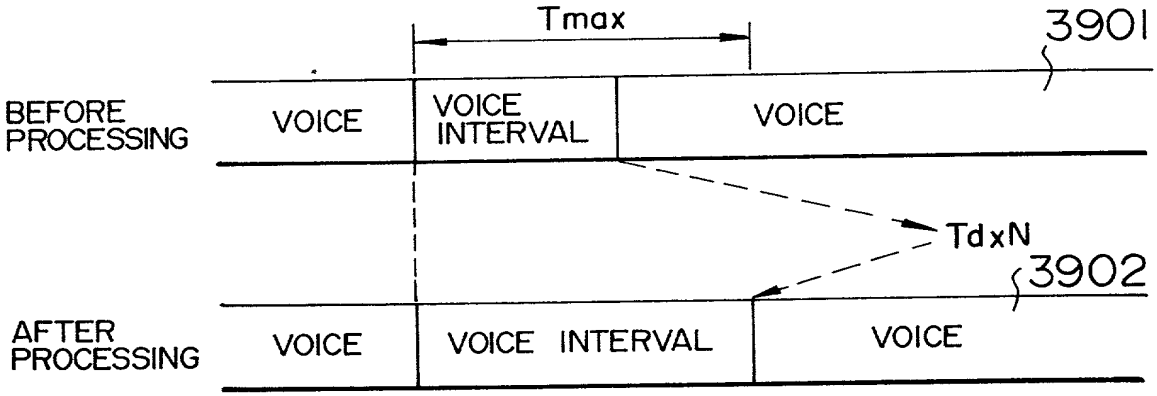

FIG. 40

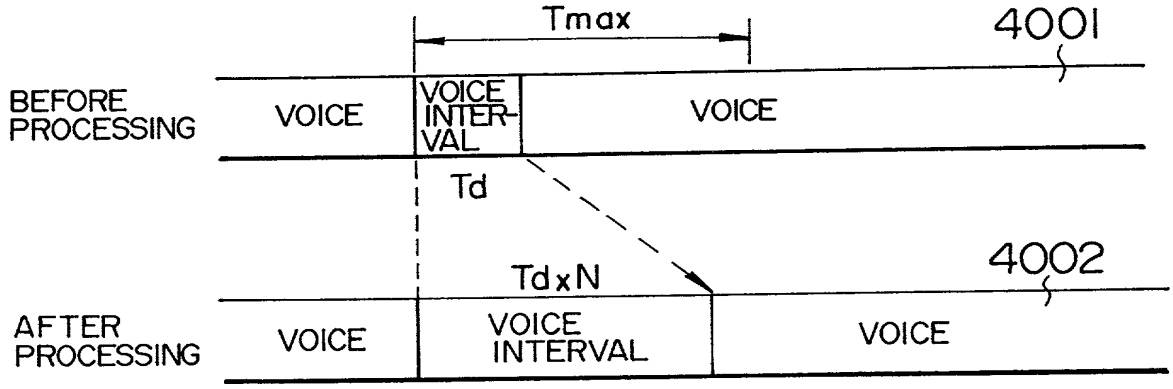

FIG. 41

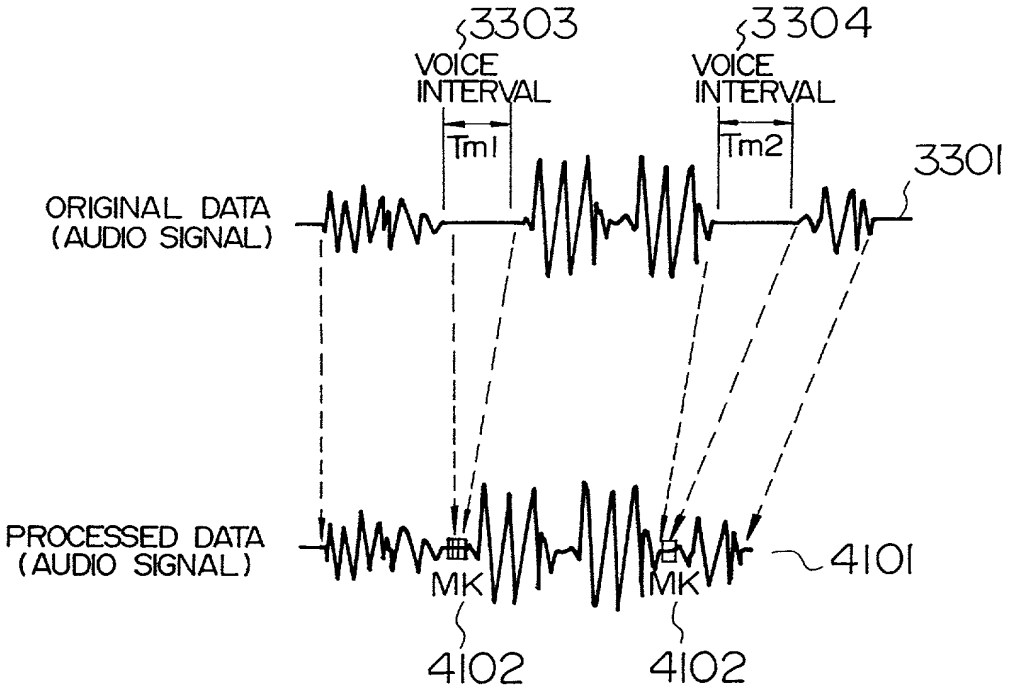
3303
3304
VOICE INTERVAL
VOICE INTERVAL
Tm1
Tm2
3301
ORIGINAL DATA (AUDIO SIGNAL)
PROCESSED DATA (AUDIO SIGNAL)
MK
MK
4101
4102
4102

FIG. 42

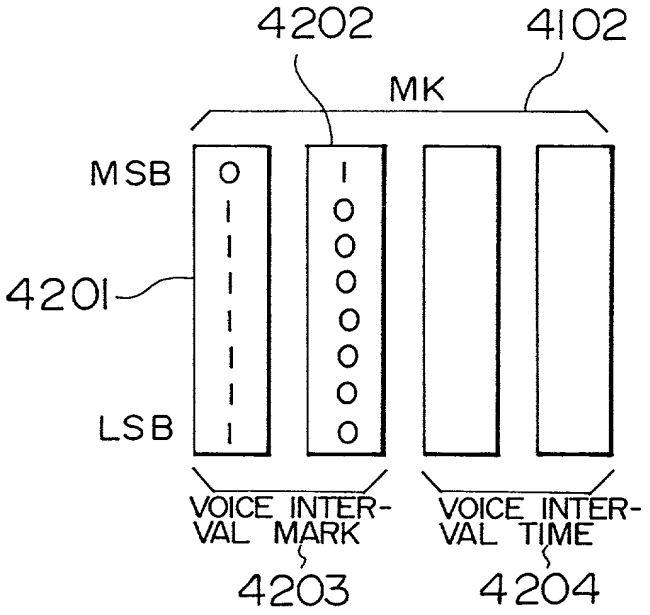
4202
4102
MK
MSB
LSB
4201
VOICE INTERVAL MARK
VOICE INTERVAL TIME
4203
4204

FIG. 43

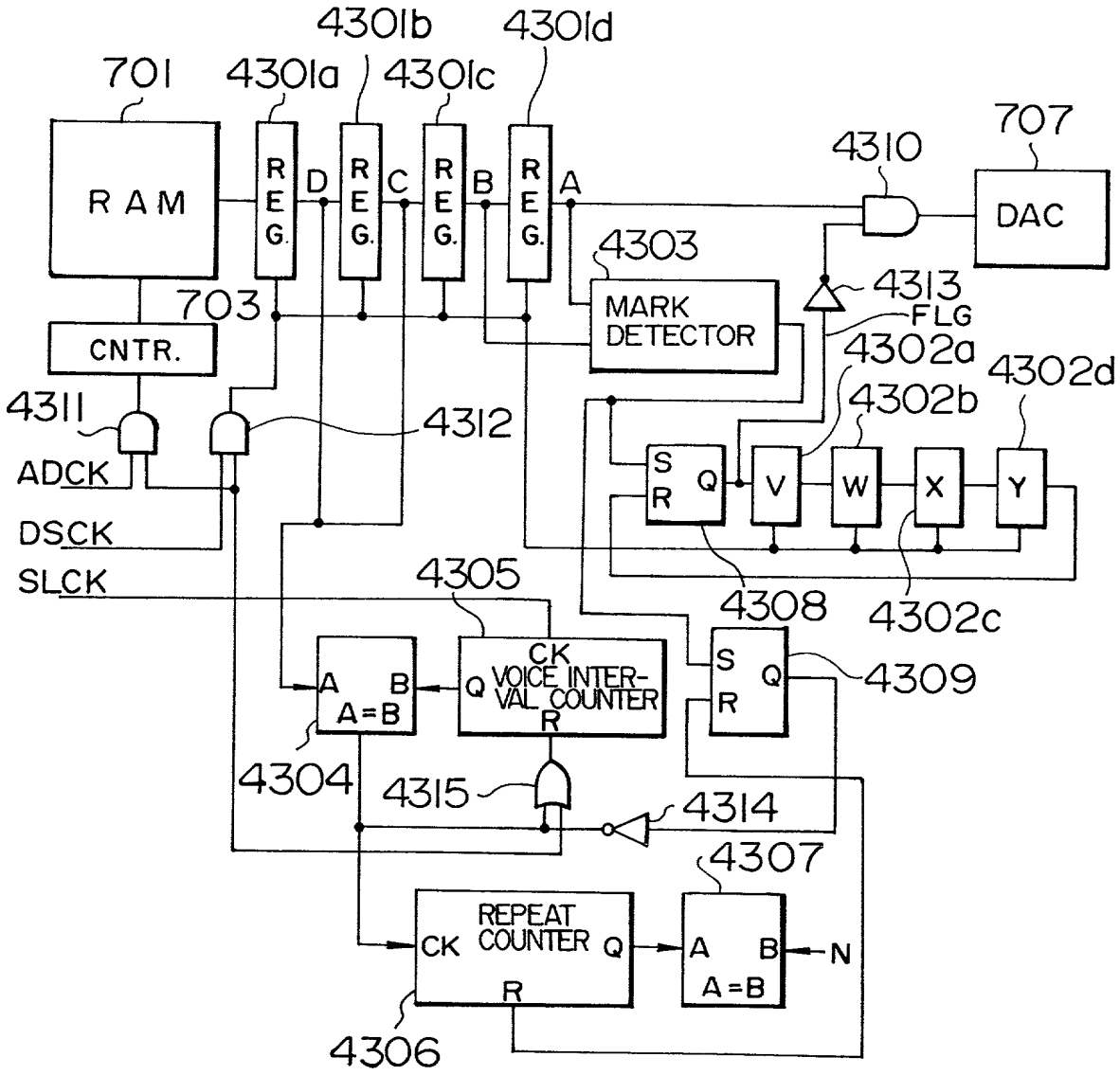
4301b
4301d
701
4301a
4301c
707
4310
RAM
REG.
D
C
B
A
DAC
4303
4313
703
MARK DETECTOR
FLG
CNTR.
4302a
4302d
4302b
4311
4312
S
R
Q
V
W
X
Y
ADCK
DSCK
SLCK
4305
4308
4302c
CK
VOICE INTER-VAL COUNTER
A
B
A=B
4309
4304
4315
4314
4307
REPEAT COUNTER
N
4306

FIG. 44

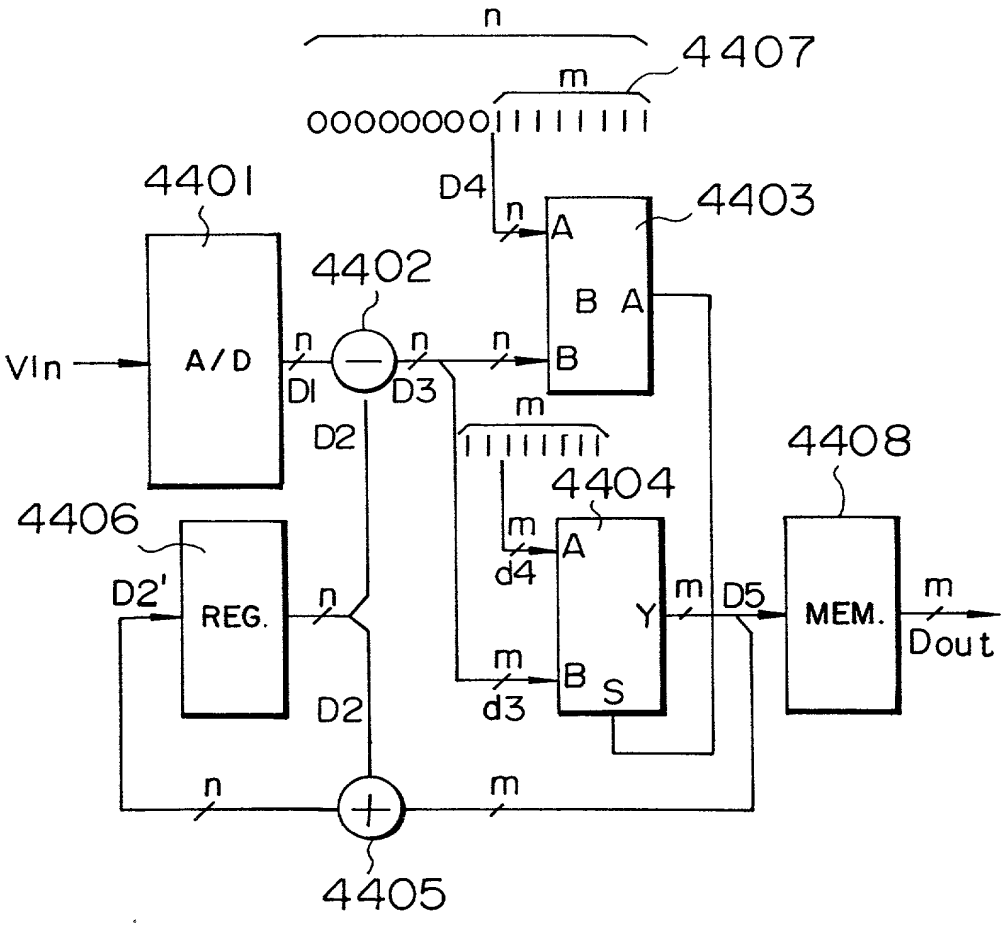
n
4407
m
00000000
4401
D4
4403
4402
A/D
Vin
DI
D3
D2
B A
A
B
m
4408
4404
4406
m
d4
D2'
REG.
n
A
Y
m
D5
MEM.
m
Dout
m
d3
B
S
D2
n
m
4405

FIG. 45

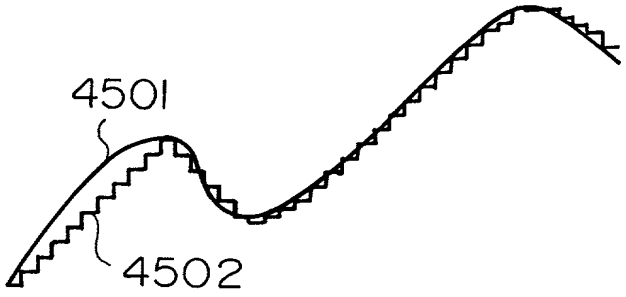
4501
4502

FIG. 46

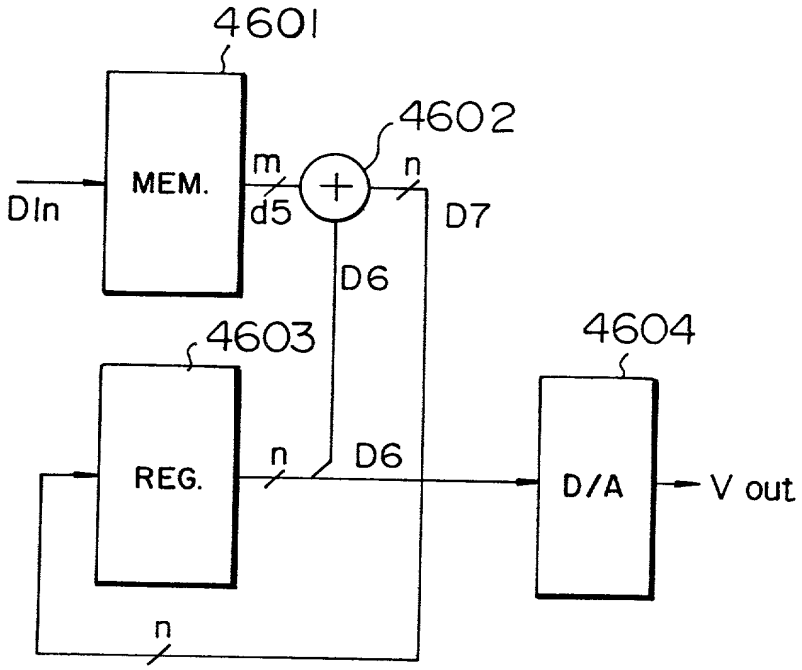
4601
4602
MEM.
DIn
m
d5
n
D7
D6
4603
4604
REG.
n
D6
D/A
V out
n

FIG. 47

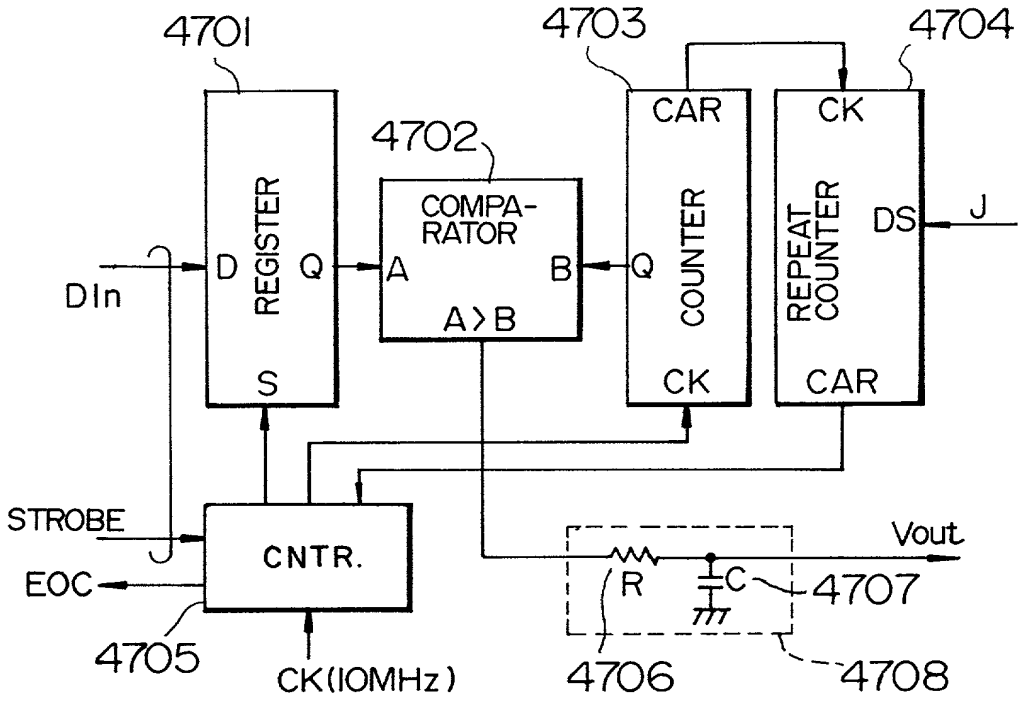
4701
4703
4704
4702
CAR
CK
COMPA-
RATOR
REGISTER
COUNTER
REPEAT
COUNTER
DS
J
DIn
D
Q
A
B
Q
A>B
S
CK
CAR
STROBE
CNTR.
Vout
EOC
R
C
4707
4705
CK(10MHz)
4706
4708

FIG. 48

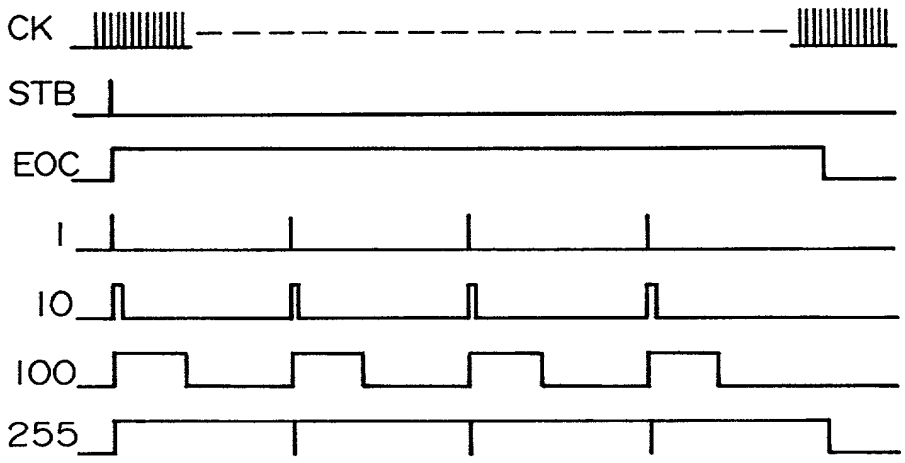
CK
STB
EOC
1
10
100
255

FIG.49

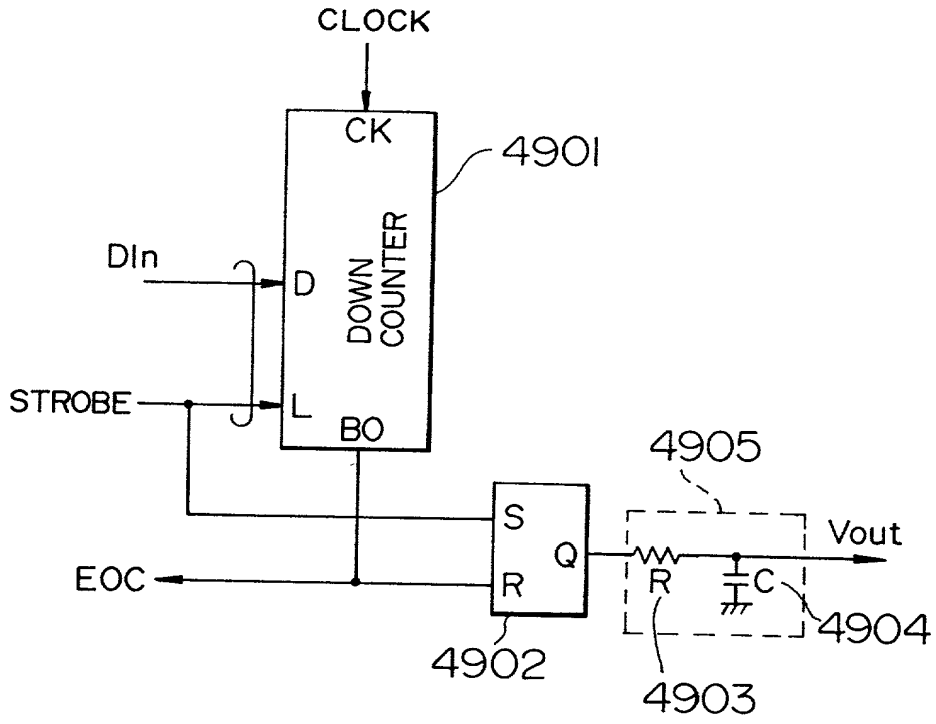
CLOCK
CK
4901
DIn
D
DOWN COUNTER
STROBE
L
BO
4905
S
Q
Vout
EOC
R
R
C
4904
4902
4903

FIG. 50

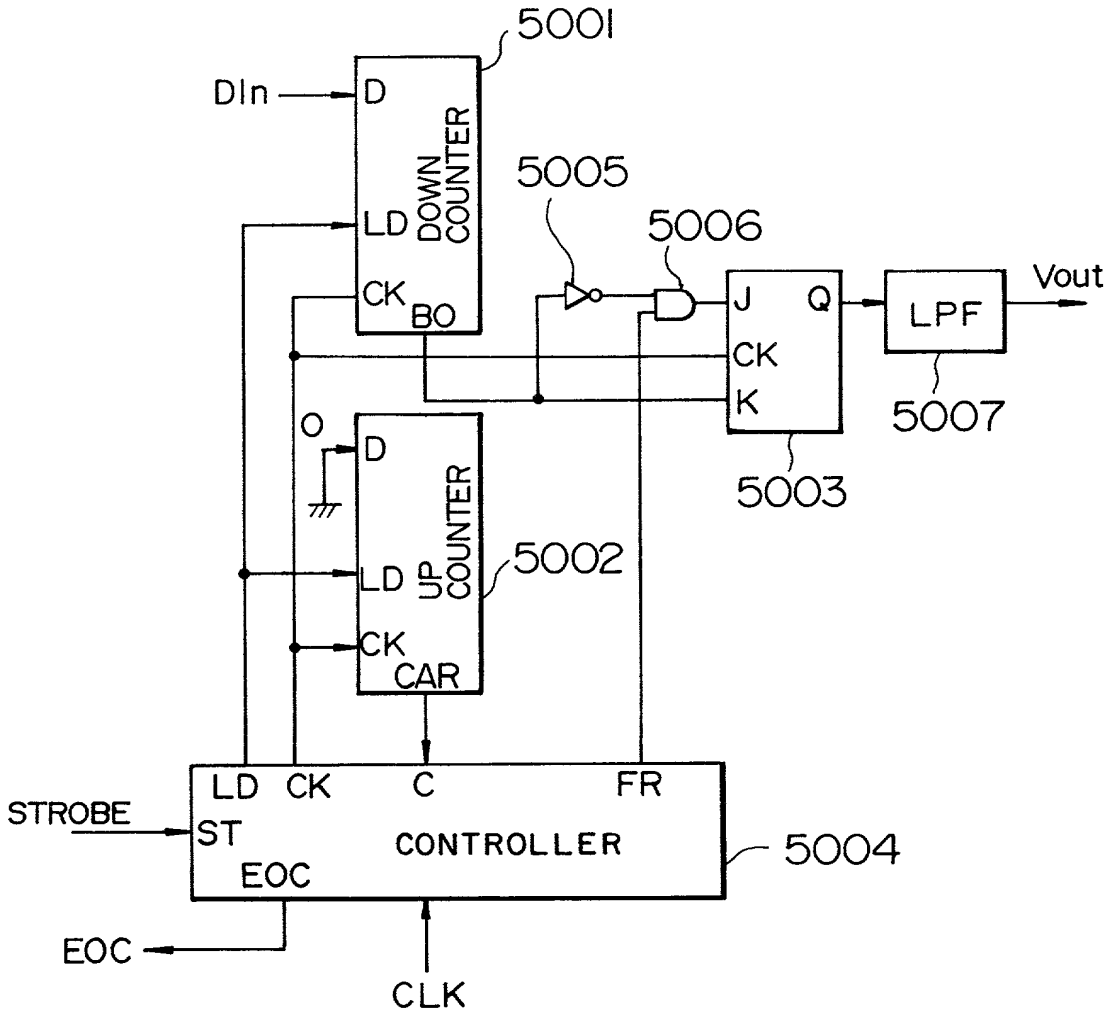
5001
DIn
D
DOWN COUNTER
LD
CK
BO
5005
5006
J
Q
CK
K
LPF
Vout
5007
5003
O
D
UP COUNTER
LD
CK
CAR
5002
LD
CK
C
FR
STROBE
ST
EOC
CONTROLLER
5004
EOC
CLK

FIG. 51

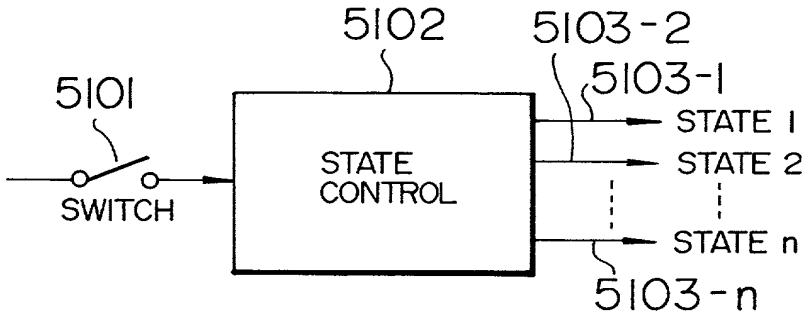

FIG. 52

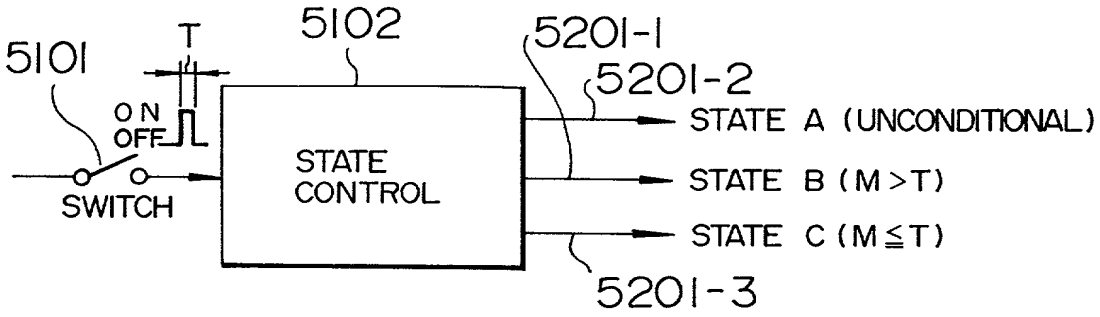

FIG. 53

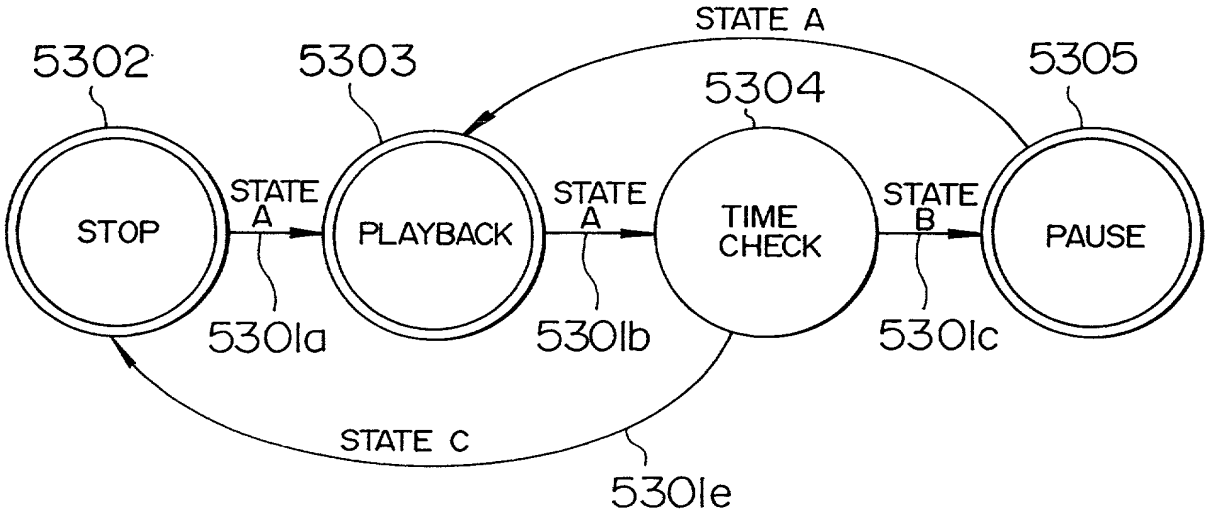

FIG. 54

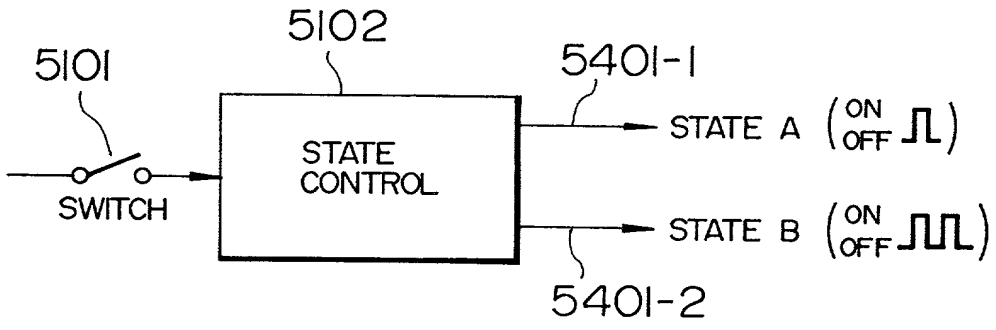
5102
5101
5401-1
STATE A (ON OFF)
STATE CONTROL
SWITCH
STATE B (ON OFF)
5401-2

FIG. 55

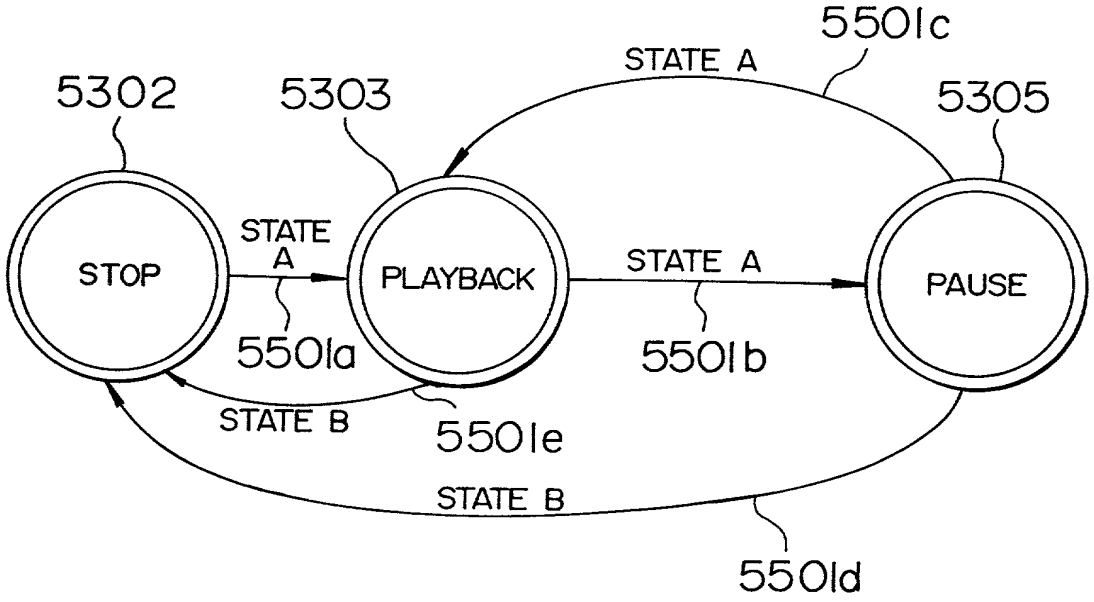
5501c
STATE A
5302
5303
5305
STOP
STATE A
PLAYBACK
STATE A
PAUSE
5501a
5501b
STATE B
5501e
STATE B
5501d

FIG. 56

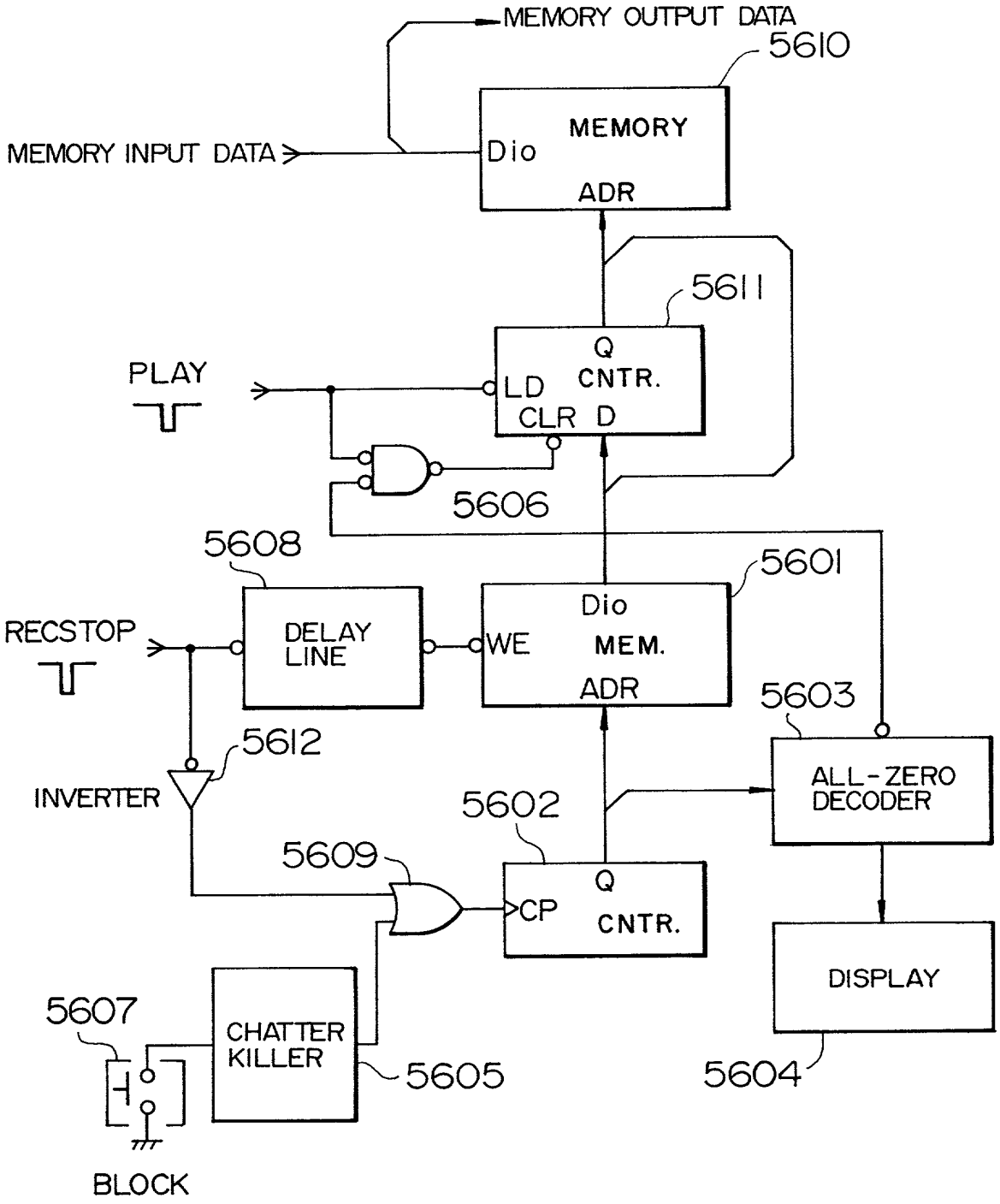
MEMORY OUTPUT DATA
5610
MEMORY
Dio
MEMORY INPUT DATA
ADR
5611
Q
CNTR.
LD
CLR
D
PLAY
5606
5608
5601
Dio
DELAY
LINE
WE
MEM.
RECSTOP
ADR
5603
5612
ALL-ZERO
DECODER
INVERTER
5602
5609
Q
CP
CNTR.
DISPLAY
5607
CHATTER
KILLER
5605
5604
BLOCK

FIG. 57

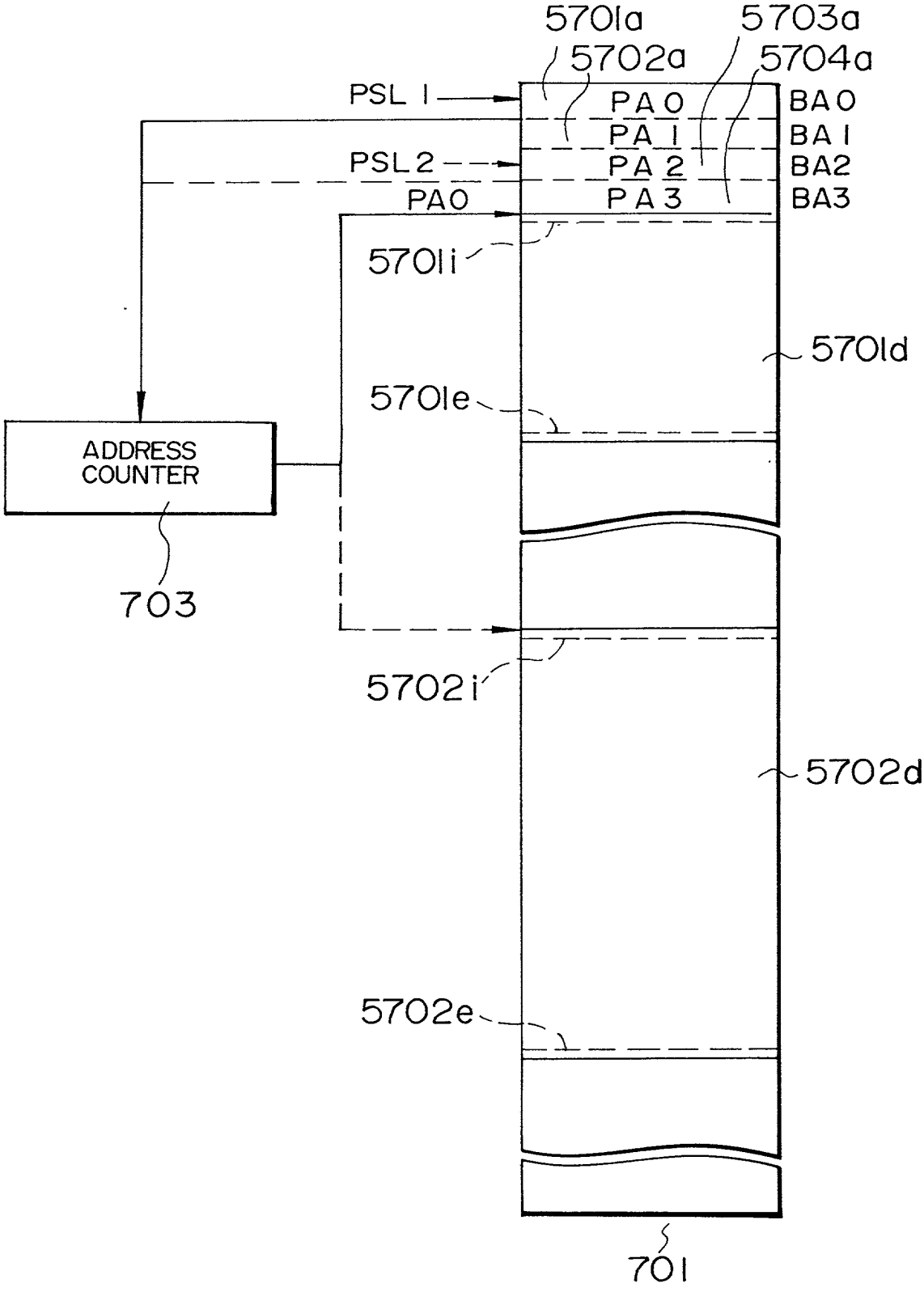
5701a
5703a
5702a
5704a
PSL 1
PSL2
PA0
PA 1
PA 2
PA 3
BA0
BA 1
BA2
BA3
5701i
5701d
5701e
ADDRESS COUNTER
703
5702i
5702d
5702e
701

FIG. 58

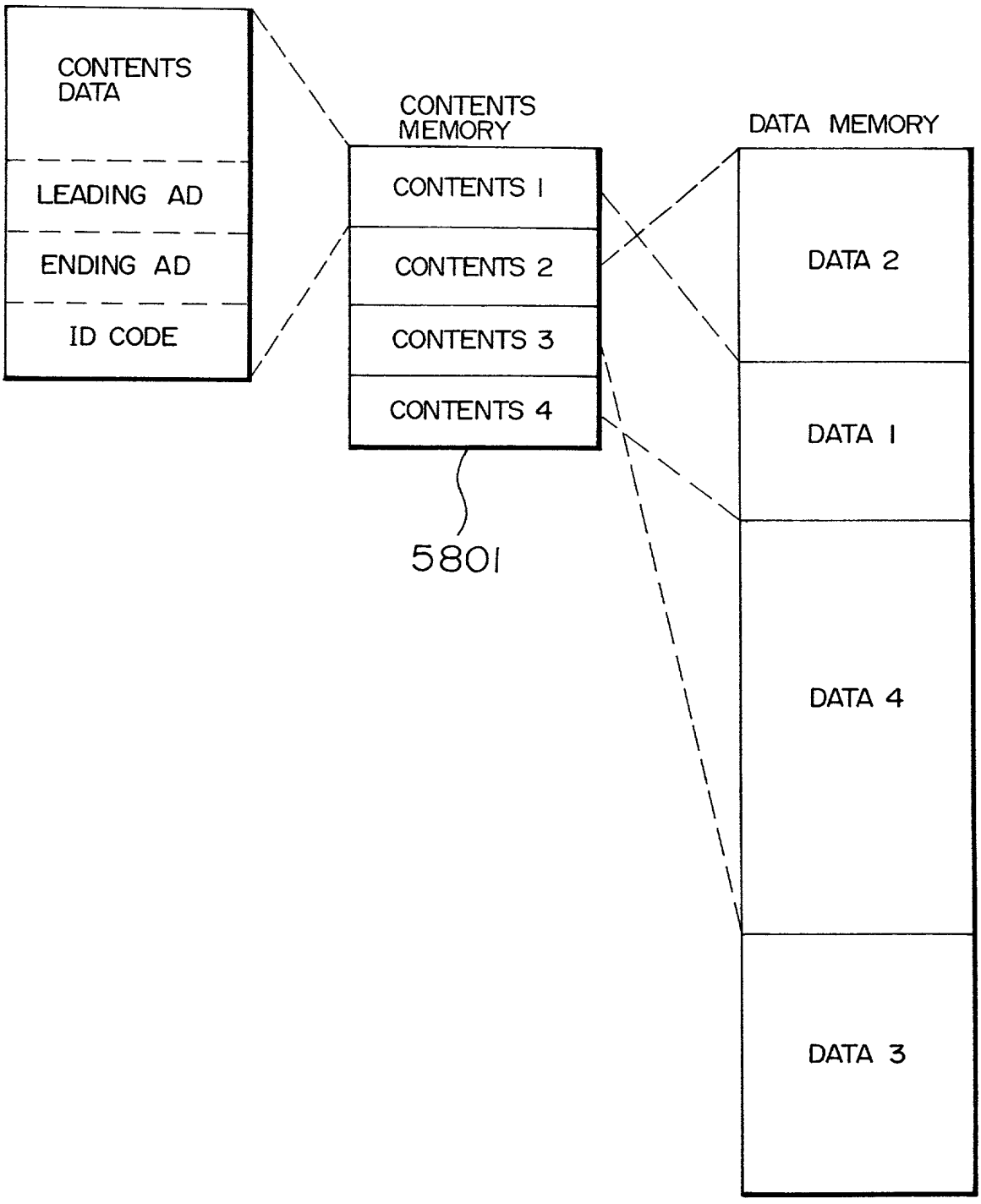
CONTENTS DATA
LEADING AD
ENDING AD
ID CODE
CONTENTS MEMORY
CONTENTS 1
CONTENTS 2
CONTENTS 3
CONTENTS 4
5801
DATA MEMORY
DATA 2
DATA 1
DATA 4
DATA 3

FIG. 59

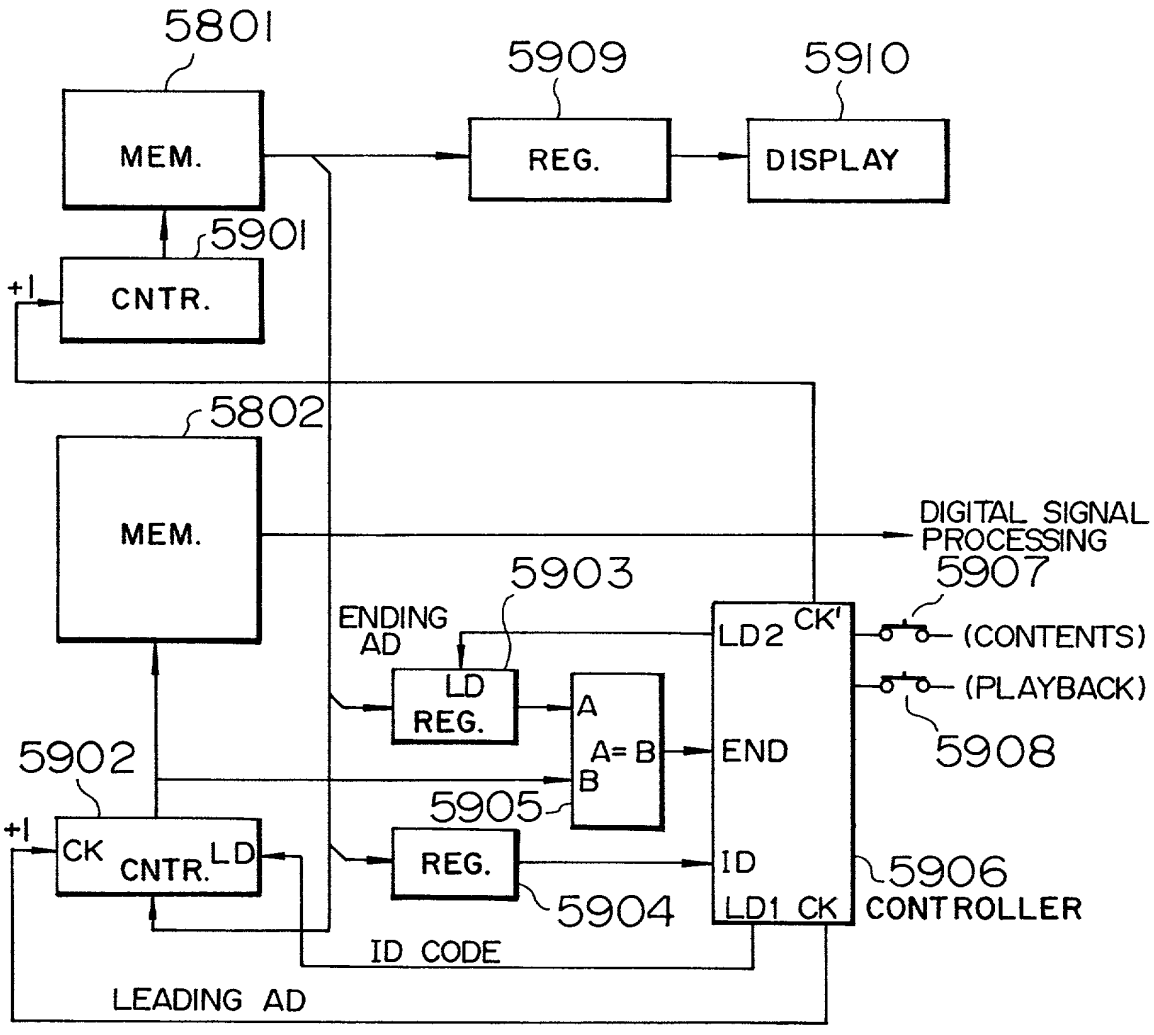
5801
MEM.
5909
REG.
5910
DISPLAY
5901
CNTR.
+1
5802
MEM.
DIGITAL SIGNAL PROCESSING
5903
ENDING AD
LD REG.
A
A=B
B
5907
LD2 CK'
(CONTENTS)
(PLAYBACK)
5908
END
5902
+1
CK CNTR. LD
5905
REG.
5904
ID
LD1 CK
5906 CONTROLLER
ID CODE
LEADING AD

FIG. 60

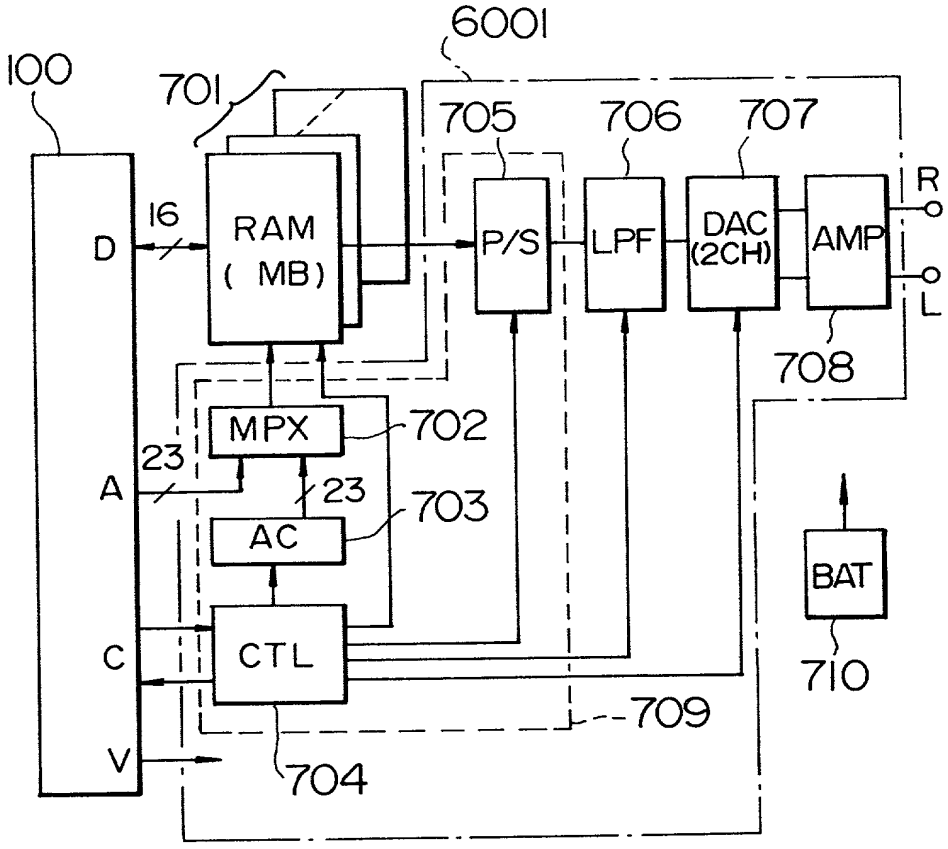
6001
100
701
705
706
707
R
L
D
16
RAM
(MB)
P/S
LPF
DAC
(2CH)
AMP
708
MPX
702
23
A
23
703
AC
BAT
C
CTL
710
709
V
704

FIG. 61

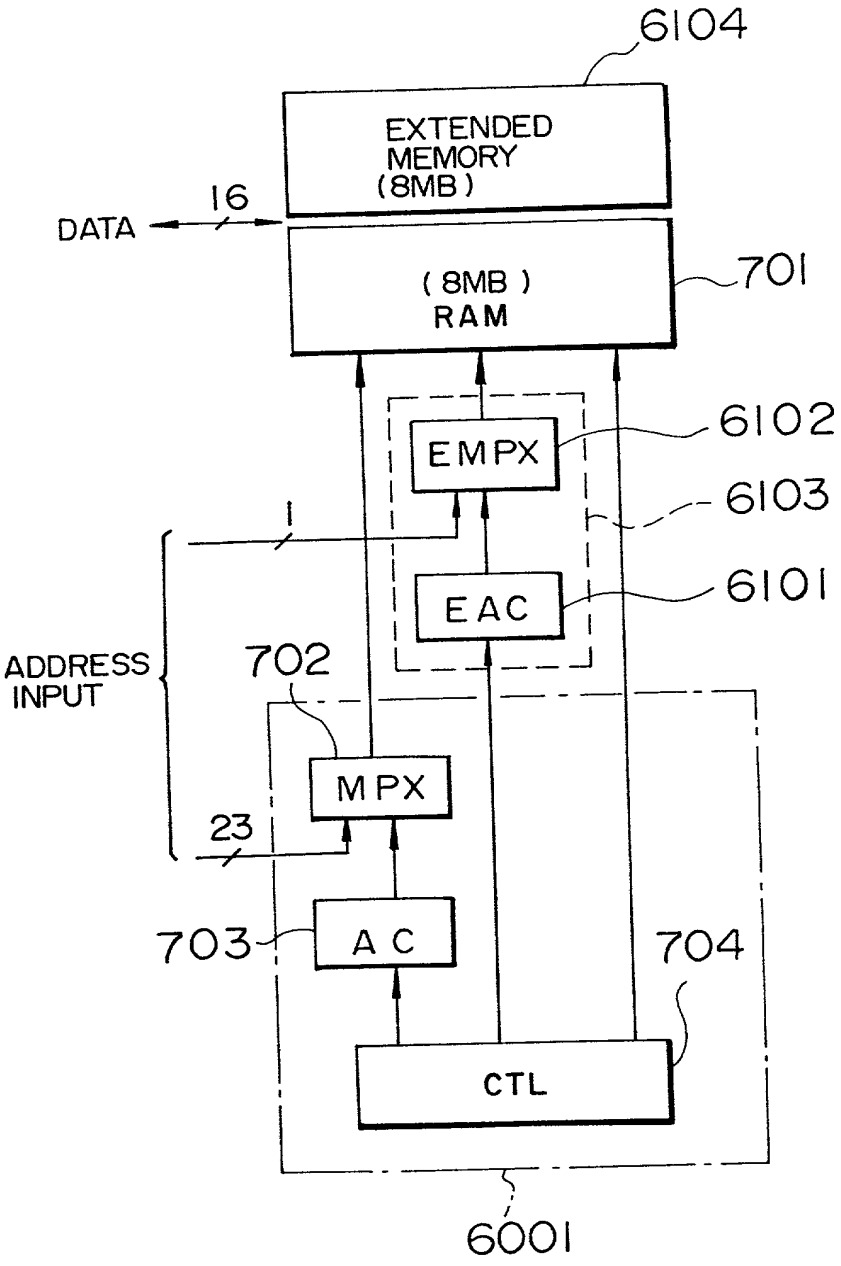
6104
EXTENDED MEMORY (8MB)
16
DATA
(8MB) RAM
701
EMPX
6102
6103
1
EAC
6101
ADDRESS INPUT
702
MPX
23
703
AC
704
CTL
6001

FIG. 62

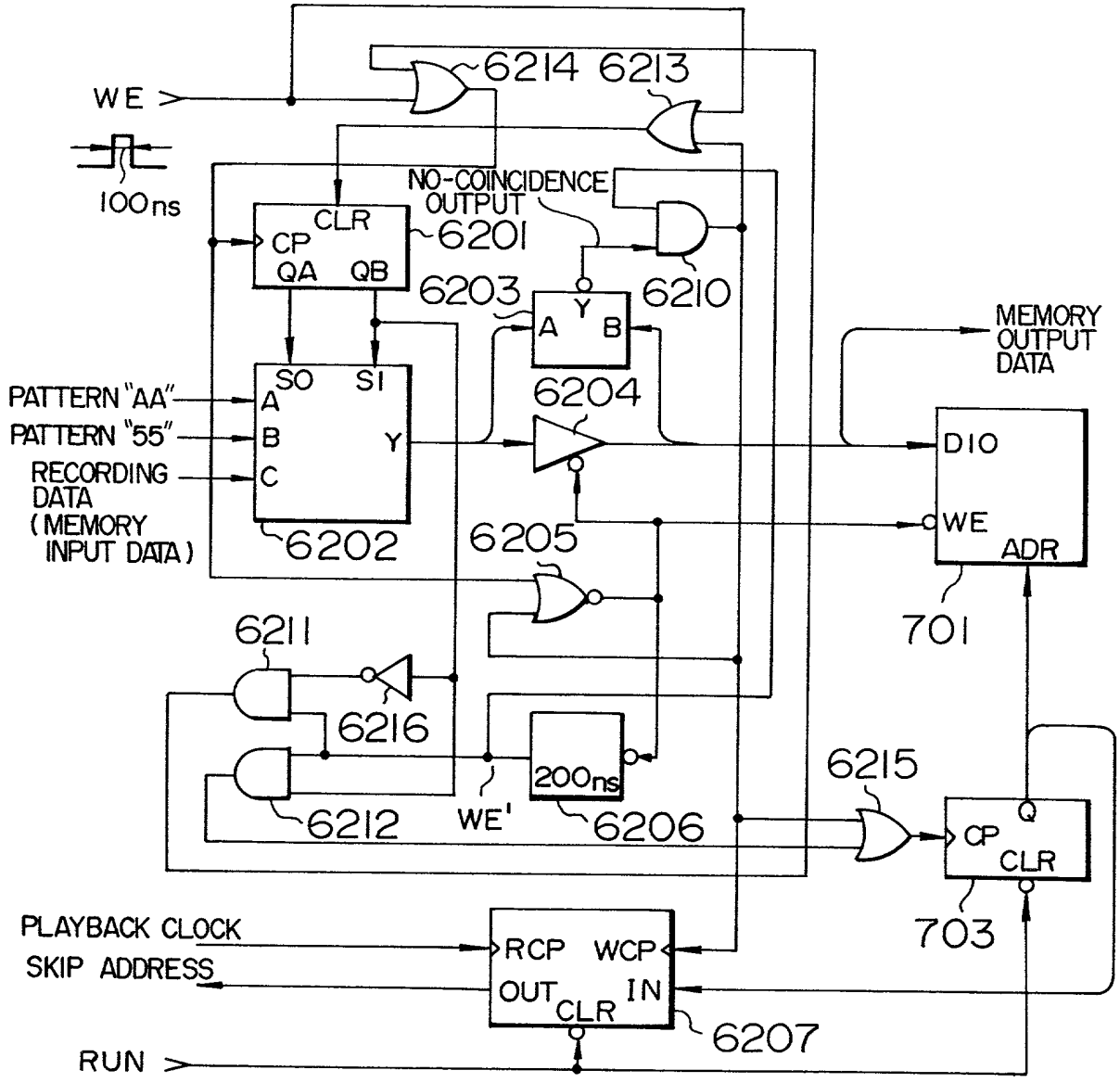
WE
100ns
6214
6213
NO-COINCIDENCE OUTPUT
CLR
CP
QA
QB
6201
6203
Y
A
B
6210
MEMORY OUTPUT DATA
PATTERN "AA"
PATTERN "55"
RECORDING DATA (MEMORY INPUT DATA)
SO
SI
A
B
C
Y
6202
6204
D10
WE
ADR
701
6205
6211
6216
6212
WE'
200ns
6206
6215
Q
CP
CLR
703
PLAYBACK CLOCK
SKIP ADDRESS
RCP
WCP
OUT
CLR
IN
6207
RUN

FIG. 63

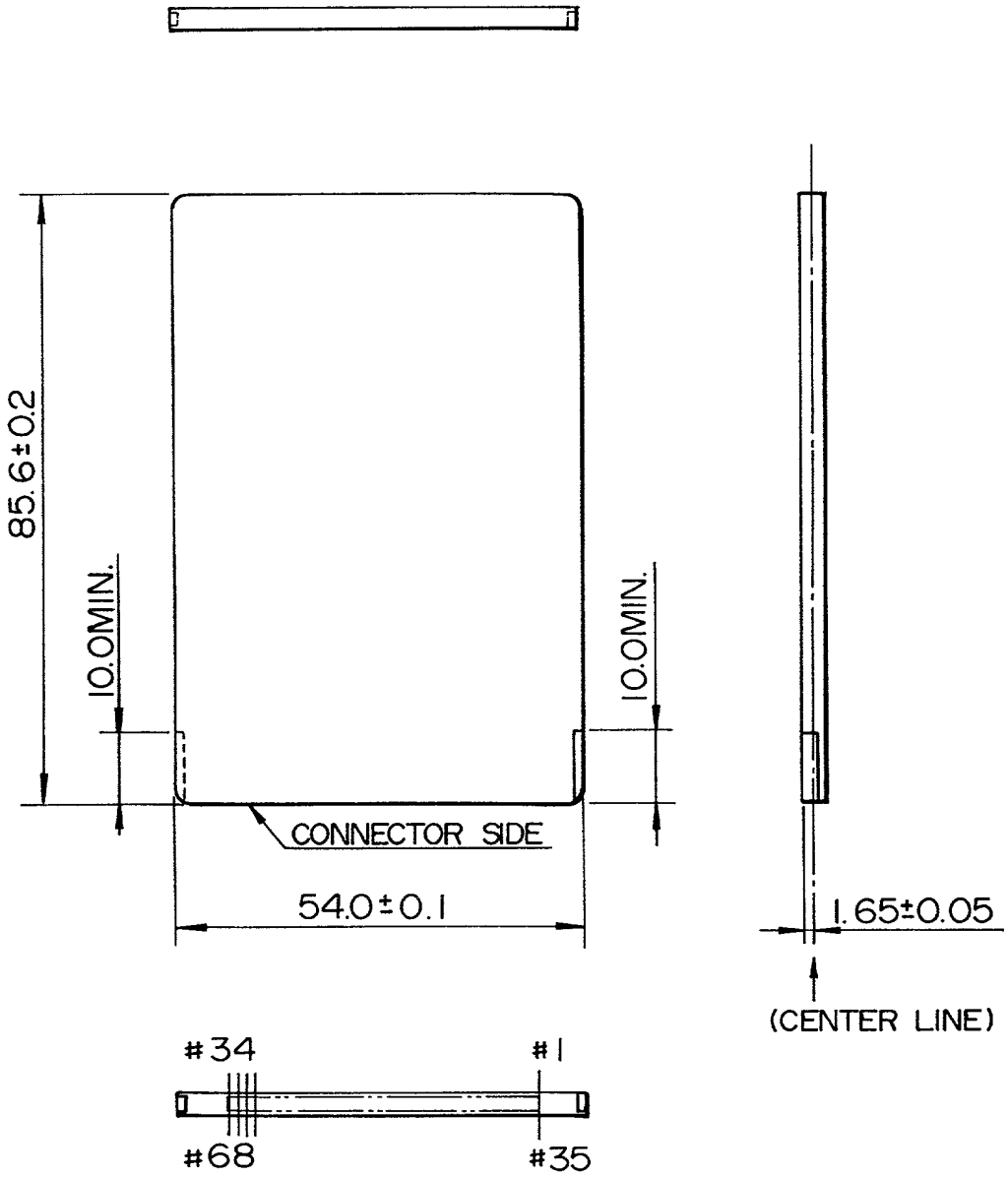
85.6±0.2
10.0MIN.
10.0MIN.
CONNECTOR SIDE
54.0±0.1
1.65±0.05
(CENTER LINE)
#34
#1
#68
#35

FIG. 64

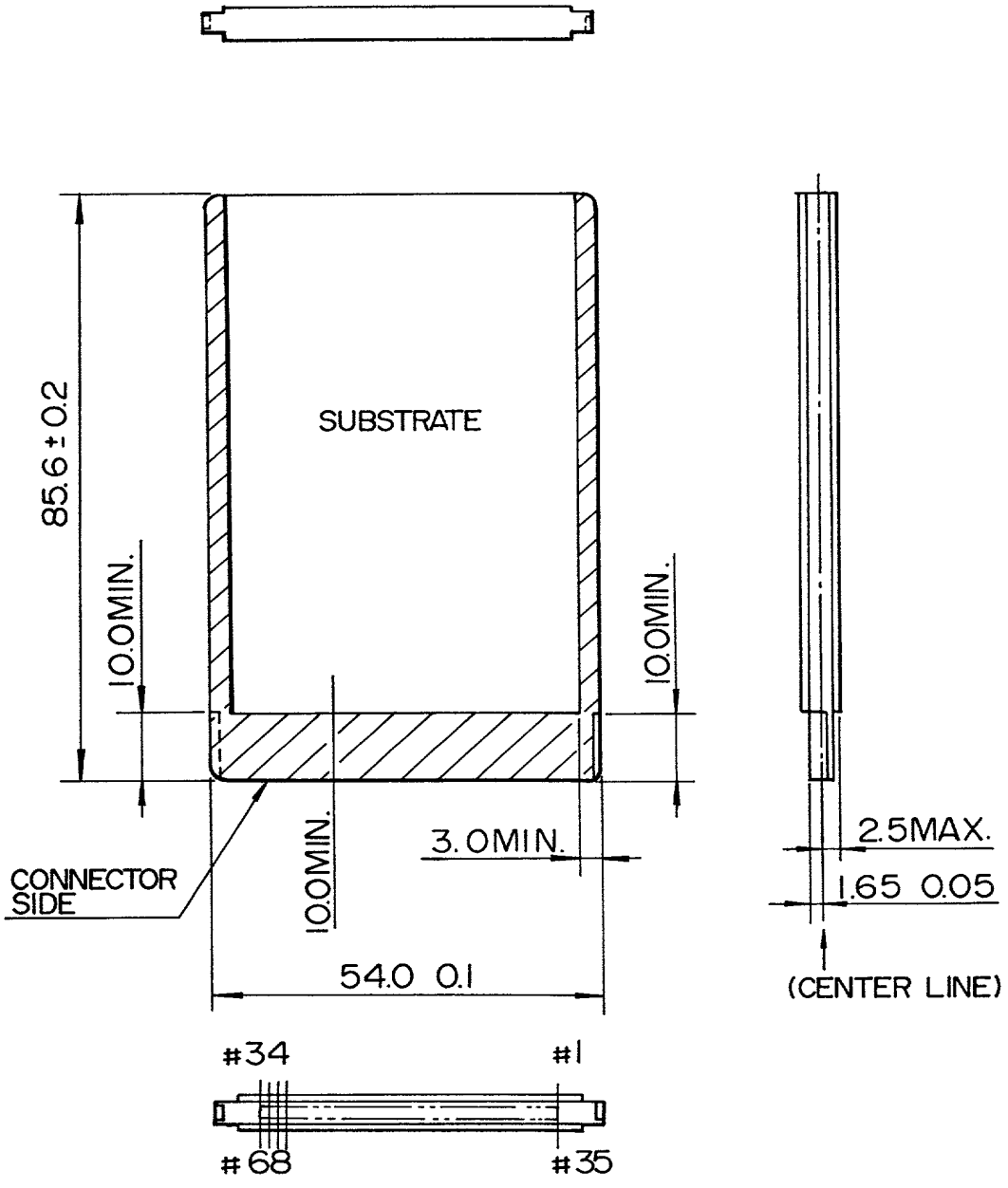
SUBSTRATE
85.6±0.2
10.0MIN.
10.0MIN.
10.0MIN.
3.0MIN.
CONNECTOR SIDE
54.0 0.1
2.5MAX.
1.65 0.05
(CENTER LINE)
#34
#1
#68
#35

FIG.65

PIN	NAME	I/O	FUNCTION	PIN	NAME	I/O	FUNCTION
1	GND			35	GND		
2	D3	I/O		36	CD1	O	CARD DETECTION
3	D4	I/O		37	D11	I/O	
4	D5	I O		38	D12	I/O	
5	D6	I/O		39	D13	I/O	
6	D7	I/O		40	D14	I/O	
7	$\overline{CE1}$	I	CARD ENABLE	41	D15	I/O	
8	A10	I		42	$\overline{CE2}$	I	CARD ENABLE
9	$\overline{OE}$	I	OUTPUT ENABLE	43	$\overline{RFSH}$	I	REFRESH (FOR PSRAM)
10	A11	I		44	RFU	NC	RESERVE
11	A 9	I		45	RFU	NC	RESERVE
12	A8	I		46	A17	I	
13	A13	I		47	A18	I	
14	A14	I		48	A19	I	
15	$\overline{WE}/\overline{PGM}$	I	WRITE ENABLE	49	A20	I	
16	RDY/$\overline{BSY}$	O	RDY $\overline{BSY}$(EEPROM)	50	A21	I	
17	VCC			51	VCC		
18	VPP1		PROGRAM POWER (EVEN-NUMBERED BYTES)	52	VPP2		PROGRAM POWER (ODD-NUMBERED BYTES)
19	A16	I		53	A22	I	
20	A15	I		54	A23	I	
21	A12	I		55	A24	I	
22	A 7	I		56	A25	I	
23	A 6	I		57	RFU	NC	RESERVE
24	A 5	I		58	RFU	NC	RESERVE
25	A 4	I		59	RFU	NC	RESERVE
26	A 3	I		60	RFU	NC	RESERVE
27	A 2	I		61	$\overline{REG}$	I	ATTRIBUTE MEMORY SELECTION
28	A 1	I		62	BVD2	O	BATTERY VOLTAGE DETECTION
29	A0	I		63	BVD1	O	
30	D0	I/O		64	D8	I/O	
31	D1	I/O		65	D9	I/O	
32	D2	I/O		66	D10	I/O	
33	WP	O	WRITE PROTECT	67	$\overline{CD2}$	O	CARD DETECTION
34	GND			68	GND		

FIG. 66

ITEM	SIGNAL	MEMORY CARD	SYSTEM	MEMORY CARD OUTPUT FORMAT
CONTROL SIGNAL	$\overline{CE1}$ $\overline{CE2}$ $\overline{REG}$	PULL UP TO VCC $R \geqq 10K\Omega$	———	———
	$\overline{OE}$ $\overline{WE}/\overline{PGM}$	PULL UP TO VCC $R \geqq 10K\Omega$, OR NO RESISTANCE	———	———
	RDY/$\overline{BSY}$	———	PULL UP	NOT DETERMINED
	$\overline{RFSH}$	NC	———	———
ADDRESS	A0-A25	PULL DOWN TO GND $R \geqq 100K\Omega$, OR NO RESISTANCE	———	———
DATA BUS	D0-D15	PULL DOWN TO GND $R \geqq 100K\Omega$, OR NO RESISTANCE	———	THREE-STATE
CARD DETECTION	$\overline{CD1}$ $\overline{CD2}$	CONNECT CARD GND	PULL UP	CONNECT TO GND IN MEMORY CARD
WRITE PROTECTION	WP	———	———	"H" OR "L"
BATTERY VOLTAGE DETECTION	BVD1 BVD2	———	PULL UP	"H" OR "L"
RESERVE PIN	RFU	NC	NC	

FIG. 67

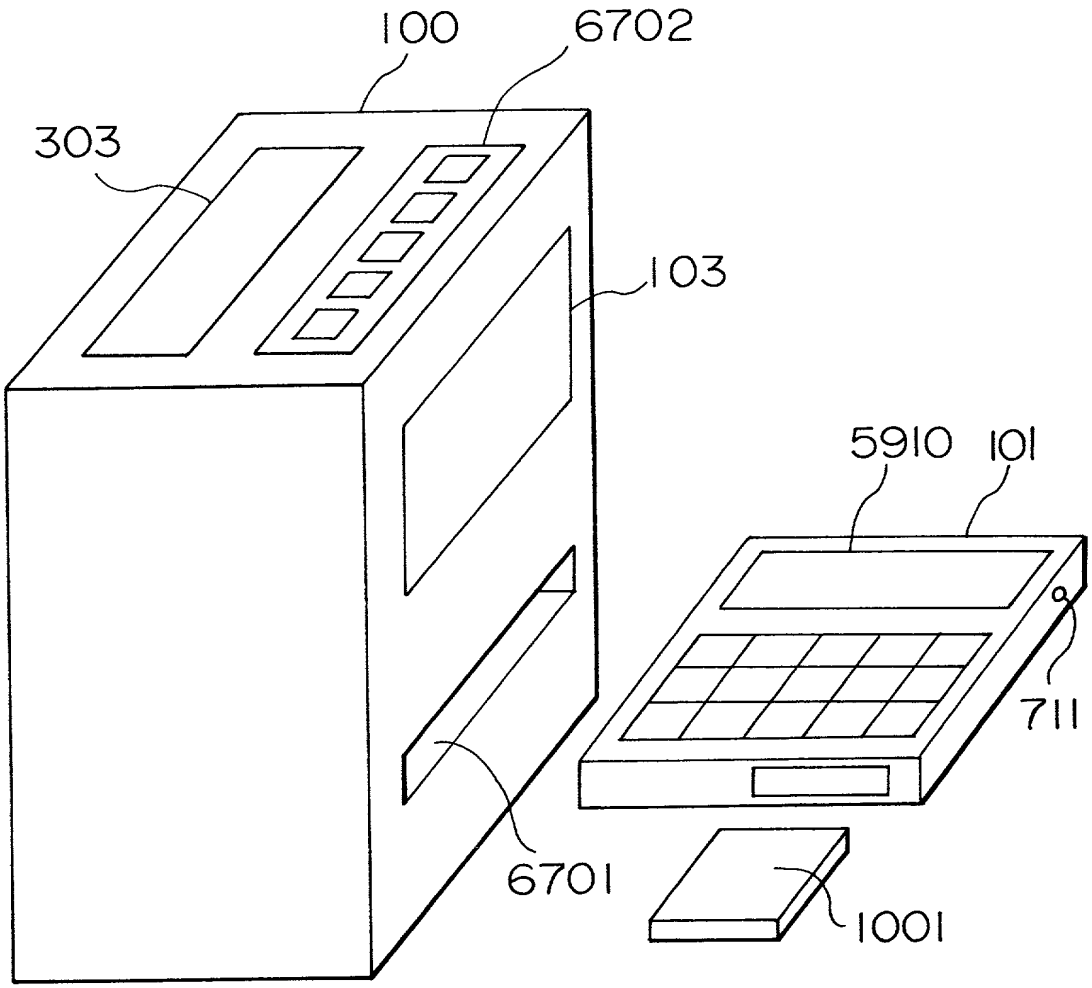

FIG. 68

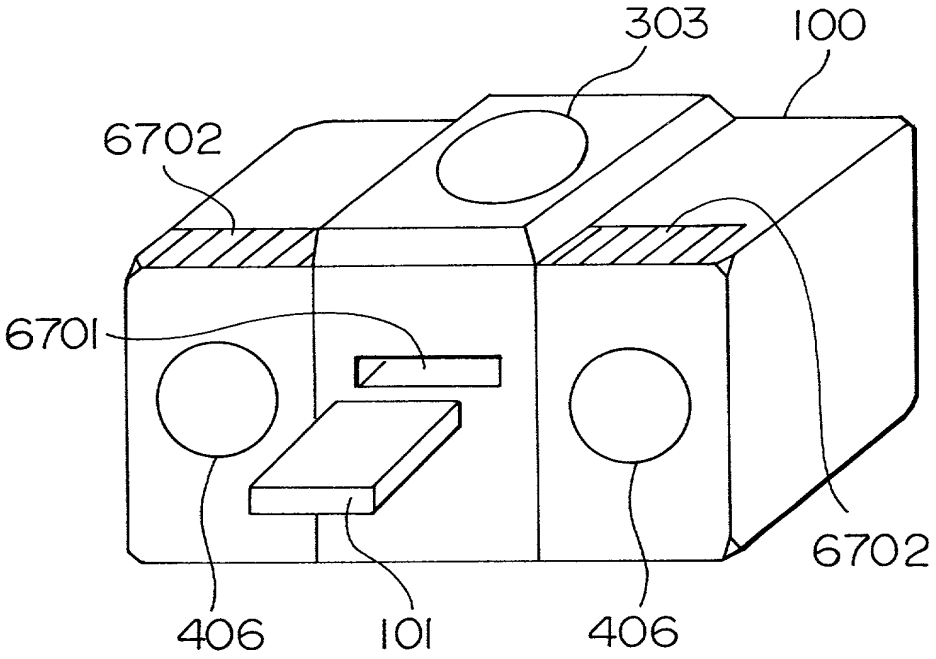

FIG. 69